

QUANTA COMPUTER INC.

(March/31/2003) Rev : E

PAG	Content	PAG	Content
1	Cover Page	31	POWER 12V_HDD & AGP(VDDQ)
2	650 System Block Diagram	32	POWER - DDR & 2.5V
3	SOCKET 478 - 1	33	SYSTEM POWER
4	SOCKET 478 - 2	34	POWER DISCHARGE
5	SOCKET 478 - 3	35	POWER CORE
6	650-1 (Host/AGP)	36	
7	650-2 (Memory for DDR)	37	
8	650-3 (HyperZip/VGA/Misc.)	38	
9	650-4 (Powers)	39	
10	962-1 (PCI/IDE/HyperZip)	40	
11	962-2 (Misc. Signals)	41	
12	962-3 (USB/1394/IPB)	42	
13	962-4 (Powers)	43	
14	Main Clock Generator & BUFFER	44	
15	AGP SLOT	45	
16	CRT,LCD LID,BLON & FAN CONTROL	46	
17	DIMM1 & DIMM2	47	
18	DDR_TERMINASION	48	
19	USB,LED/B,PS2,PW & RST CONN	49	
20	PCI CONN & PULL UP	50	
21	LAN PHY (AC101L) & RJ45,RJ11	51	
22	IDE (HDD & CDROM) & LPT	52	
23	1394(RTL8801B)	53	
24	HOLE,EMI,RTC & COM1	54	
25	SUPER_I/O & BIOS ROM	55	
26	AUDIO CODEC(ALC650)	56	
27	AUDIO AMPLIFIER(LM4873 & 4871)	57	
28	EC W83L950D	58	
29	AUDIO DJ (0Z263)	59	
30	BATTERY CONN & POWER JACK	60	

VB Board

or

AGP Board

Video Bridge
sis/ 302LVGraphic Chip
ATi or nVIDIA

DT1

CPU
INTEL P4
(SOCKET-478)
PAGE : 03,04,05Host Bus
(400/533MHz)AGP Connector
PAGE 15

AGP 4X BUS

Y/C

RGB

S-Video
PAGE 20CRT
PAGE 16

RGB

NORTH BRIDGE
SIS M650
(BGA 702)
PAGE : 06,07,08,09266/333MHz
DDR SDRAML
O
N
G
-
D
I
M
ML
O
N
G
-
D
I
M
M2*CPU/CPU-
1*SDRAM
2*HyperZip
1*AGP
4*PCI
3*REF
1*48MHz
0*24/48MHzMain
CLOCK
GEN.
PAGE : 14CLK_IN
6*CLK_OUT/-
FB_OUT
FB_INDDR
CLOCK
BUFFER
PAGE : 14MUTIO
533MHzHDD
PAGE 22

SECONDRY IDE

CDROM
PAGE 22

PRIMARY IDE

SOUTH BRIDGE
SIS 962
(BGA 371)
PAGE : 10,11,12,13

USB

Card Reader
Connector
PAGE 19USB4
PAGE 19USB2
PAGE 19USB5
PAGE 19USB3
PAGE 19BIOS
PAGE 25LED Board
Connector
PAGE 19Keyboard
Connector
PAGE 28

KEY MATRIX

PS2

Touchpad Board
Connector
PAGE 19KB/MS
PAGE 19LPT
PAGE 22COM
PAGE 24Super IO
SMSC/
LPC47M192
PAGE 25FDD
PAGE 25FAN1
PAGE 16FAN2
PAGE 16

LPC

PCI
AC97
USB 1PCI Board
Connector
PAGE 20

PCI

Card Bus
O2/ OZ6912PCMCIA
SlotMini-PCI
Slot

MDC Slot

LAN PHY
Broadcom/ AC101L
PAGE 21RJ45
PAGE 211394 PHY
Agere/ FW802C
PAGE 231394
PAGE 231394
PAGE 23Audio DJ
O2/ OZ263
PAGE 29Audio DJ Board
Connector
PAGE 29Audio Codec
Realtek/ ALC202
PAGE 26MIC-IN
PAGE 26Audio Amp
NS/ LM4873LQ
PAGE 27Headphone
PAGE 27Audio Amp
NS/ LM4871LD
PAGE 27Speaker
PAGE 27Sub-woofer
PAGE 27

RTCVDD

Power

RTC
PAGE : 24

VIN

BATTERY & ACIN
PAGE : 30

VA2

VAD

VDDQ

12V & VDDQ
PAGE : 31

12V_HDD

VCC2_5_M

VCC2_5_MEM

DDR_VTT

DDR & 2.5V
PAGE : 32

5VPCU

3VPCU

+5VSUS

+3VSUS

5V

12VOUT

3V

SYSTEM POWER
PAGE : 33

1.8VSUS

1.8V

POWER DISCHARGE
PAGE : 34

VCCP

VCCVID

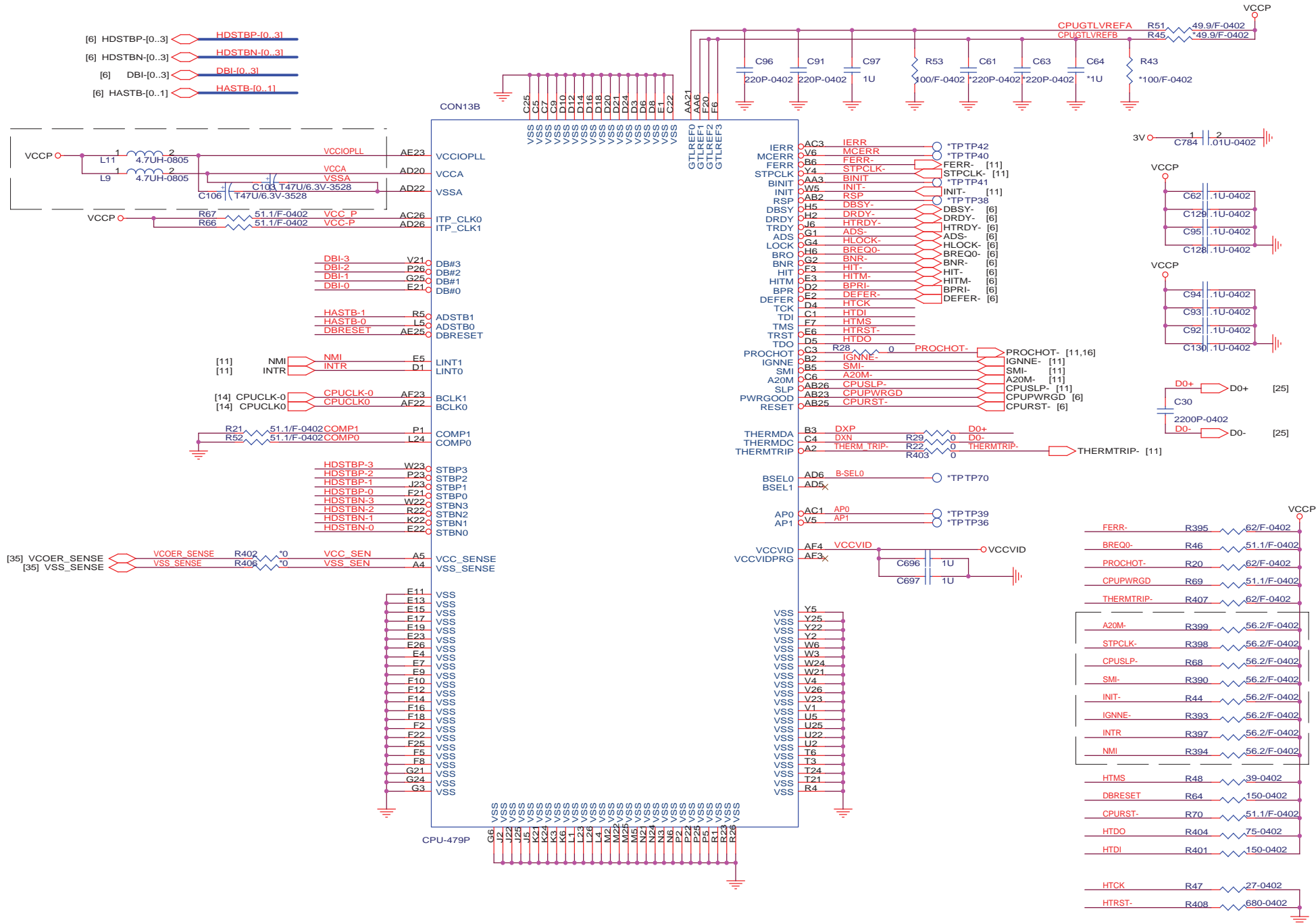
DDR_VTT

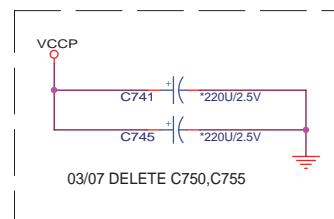
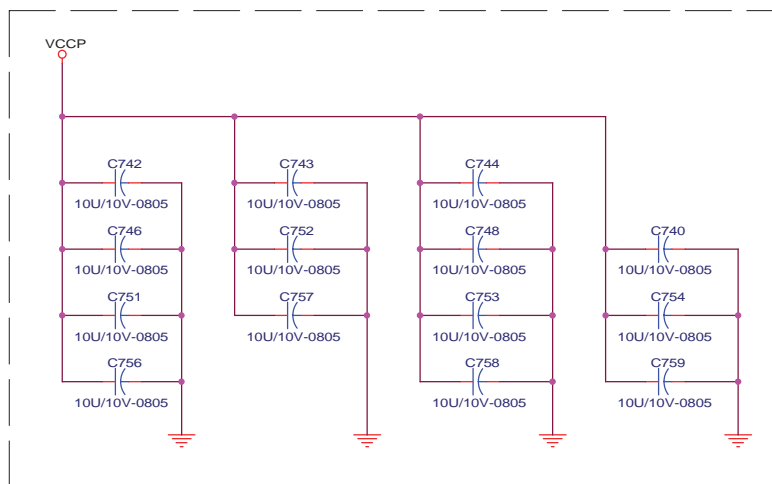
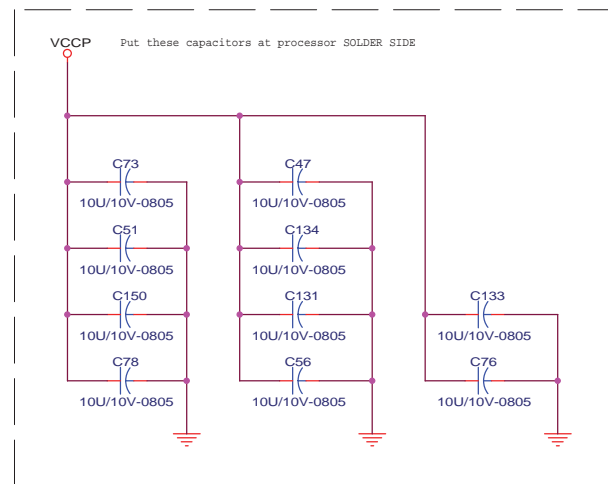
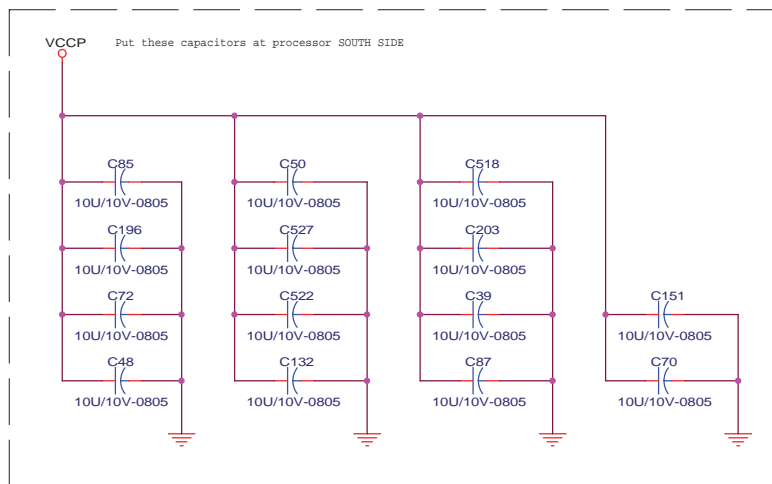
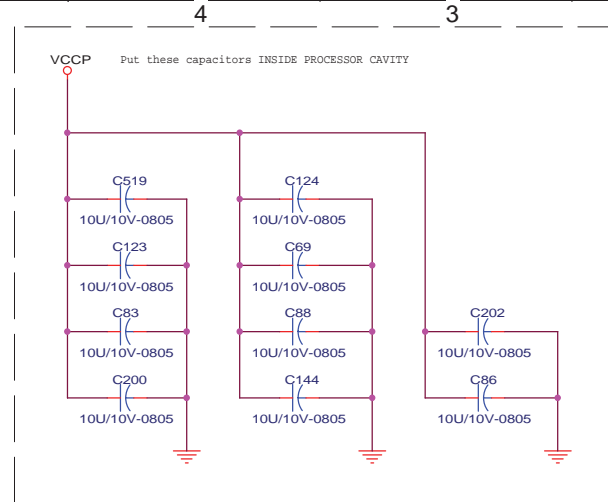
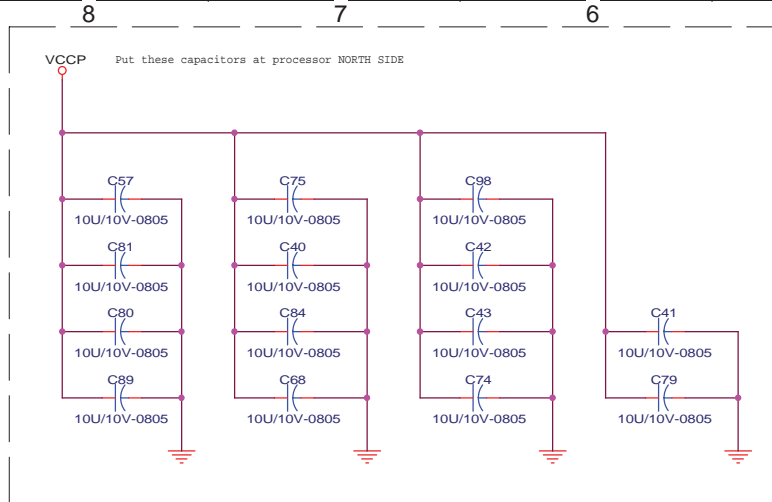
POWER CORE
PAGE : 35PROJECT : DT1
Quanta Computer Inc.

Size Custom	Document Number BLOCK DIAGRAM	Rev E
Date: Friday, April 04, 2003	Sheet 2 of 35	

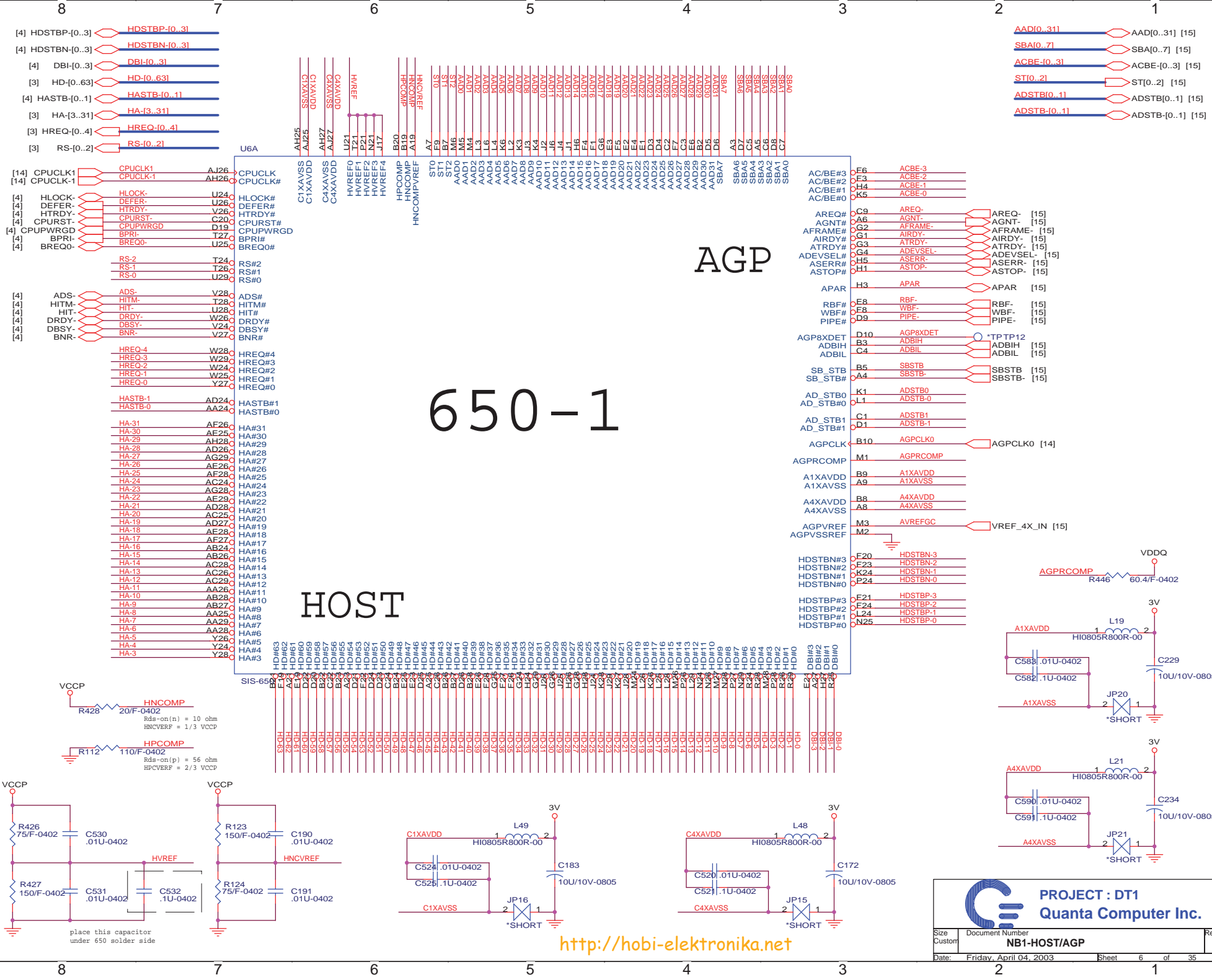
<http://hobi-elektronika.net>





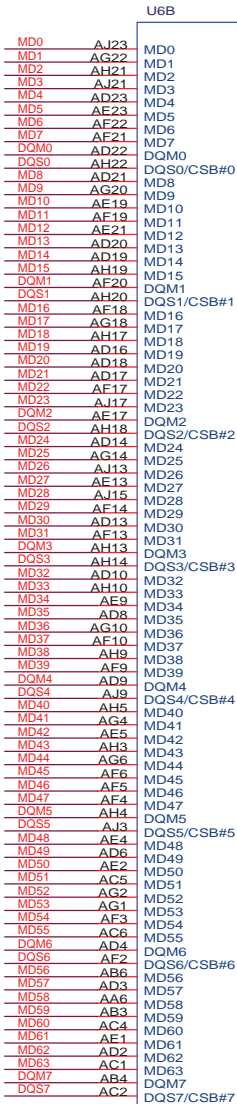
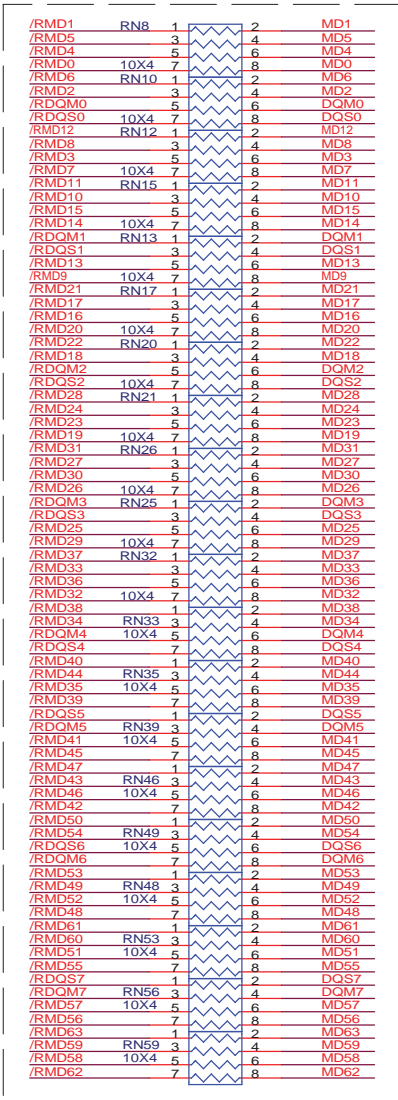


P.S. Choose X7R/X5R components instead of Y5V for all 10uF_1206 capacitors on this page.



/RMD[0..63] [17,18]
 /RDQM[0..7] [17,18]
 /RDQS[0..7] [17,18]
 /RMA[0..14] [17,18]
 /RCS-[0..5] [17,18]
 /CKE[0..3] [17,18]

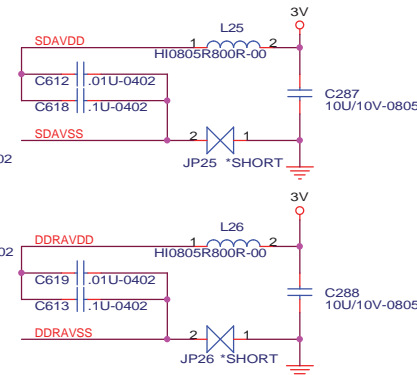
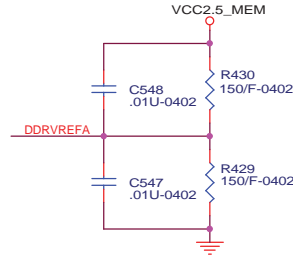
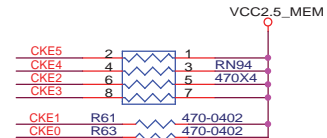
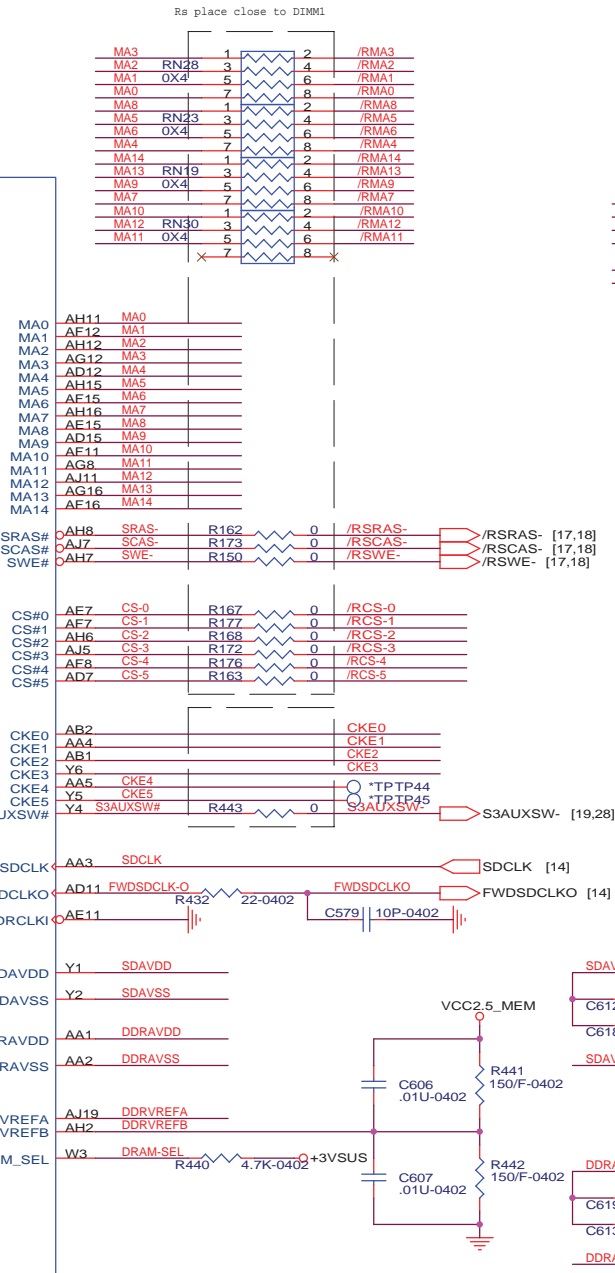
Rs place close to DIMM1



U6B

650-2

SIS-650



NOTE: This page is for universal PCB design(suitable for both 645 or 650)

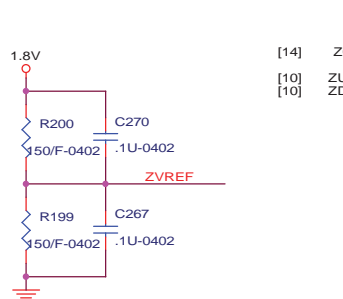
NB Hardware Trap Table

	0	1	Default	embedded pull-low (30-50K Ohm)
DLEN#	enable PLL	disable PLL	0	yes
DRAM_SEL	SDR	DDR	1(DDR)	yes
TRAP0	normal	NB debug mode	0	yes
TRAP1	TV selection, NTSC/PAL(0/1)			0
CSYNC	enable VB		0	
RSYNC	enable VGA interrupt		1	
LSYNC	enable panel link		0	

[10] ZAD[0..15] ZADI[0..15]

[10] ZSTB[0..1] ZSTBI[0..1]

[10] ZSTB-[0..1] ZSTB-[0..1]



[14] ZCLK0 ZCLK0 V3 ZCLK

[10] ZUREQ ZUREQ U6 ZUREQ

[10] ZDREQ ZDREQ U1 ZDREQ

ZSTB0 T3 ZSTB0

ZSTB-0 T1 ZSTB#0

ZSTB1 P1 ZSTB1

ZSTB-1 P3 ZSTB#1

ZAD0 T4 ZAD0

ZAD1 R3 ZAD1

ZAD2 T5 ZAD2

ZAD3 T6 ZAD3

ZAD4 R2 ZAD4

ZAD5 R6 ZAD5

ZAD6 R1 ZAD6

ZAD7 P4 ZAD7

ZAD8 R4 ZAD8

ZAD9 N3 ZAD9

ZAD10 P5 ZAD10

ZAD11 P6 ZAD11

ZAD12 N1 ZAD12

ZAD13 N6 ZAD13

ZAD14 N2 ZAD14

ZAD15 N4 ZAD15

ZVREF U3 ZVREF

VDDZCMP V5 VDDZCMP

ZCMP_N U4 ZCMP_N

ZCMP_P U2 ZCMP_P

VSSZCMP V6 VSSZCMP

Z1XAVDD W1 Z1XAVDD

Z1XAVSS W2 Z1XAVSS

Z4XAVDD V2 Z4XAVDD

Z4XAVSS V1 Z4XAVSS

VGA

Stereo Glass

HyperZip

650-3

SIS-650

[10,15,20,21,22,25,28,29] PCIRST- PCIRST- [11,28] PWRGD PWRGD [11,24] AUXOK AUXOK

VOSC1 C15 REFCLK0 REFCLK0 [14]

ROUT A12 R-OUT R438 BK1608LL680 ROUT [16]

GOUT B13 G-OUT R437 BK1608LL680 GOUT [16]

BOUT A13 B-OUT R436 BK1608LL680 BOUT [16]

HSYNC E13 H-SYNC R434 BK1005LL121 HSYNC [16]

VSNC E13 V-SYNC R433 BK1005LL121 VSNC [16]

DDC1CLK D13 DDC1-CLK R435 BK1005LL121 DDC1CLK [16]

DDC1DATA D12 DDC1-DATA R439 BK1005LL121 DDC1DATA [16]

INT#A B11 INT-A INT-A [10,15,20]

CSYNC E12 CSYNC

RSYNC A11 RSYNC

LSYNC E12 LSYNC

VCOMP E14 VCOMP

VRSET D14 VRSET

VVBWN E14 VVBWN

DACAVDD1 B12 DACAVDD

DACAVSS1 C12 DACAVSS

DACAVDD2 C13 DACAVDD

DACAVSS2 C14 DACAVSS

DCLKAVDD B15 DCLKAVDD

DCLKAVSS A15 DCLKAVSS

ECLKAVDD B14 ECLKAVDD

ECLKAVSS A14 ECLKAVSS

ROUT C603 *.1U-0402

GOUT C602 *.1U-0402

BOUT C601 *.1U-0402

HSYNC C593 *.1U-0402

VSNC C592 *.1U-0402

RSYNC 1 2

CSYNC 3 4 RN42

LSYNC 5 6 4.7KX4

DLEN- 7 8

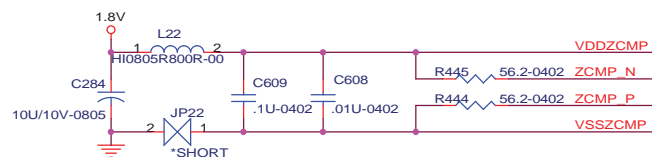
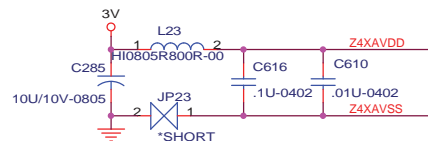
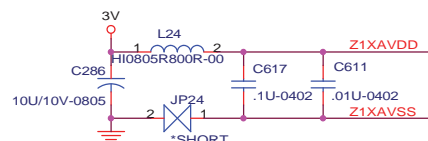
TRAP0 1 2 RN45

TRAP1 3 4

ENTEST 5 6 4.7KX4

PWRGD C261 .1U-0402

AUXOK C620 .1U-0402



PCIRST# PCIRST#

PWRGD# PWRGD#

AUXOK# AUXOK#

TRAP0 D11 TRAP0

TRAP1 D10 TRAP1

TESTMODE2 E10 TESTMODE2

TESTMODE1 E11 TESTMODE1

TESTMODE0 E12 TESTMODE0

DLEN- E13 DLEN-

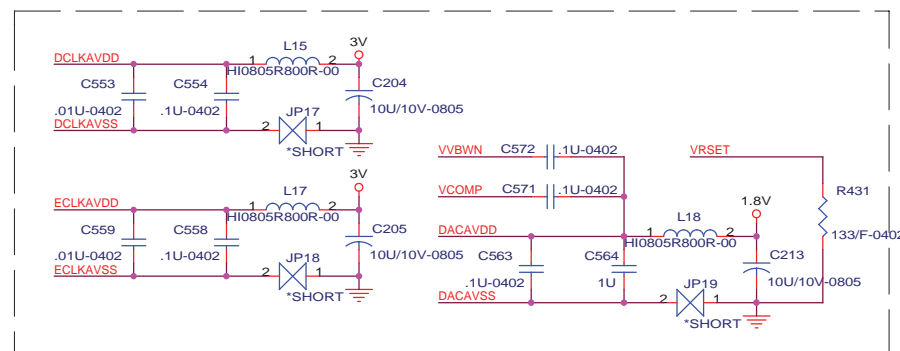
DLEN# E10 DLEN#

ENTEST E11 ENTTEST

*TPTP10

*TPTP43

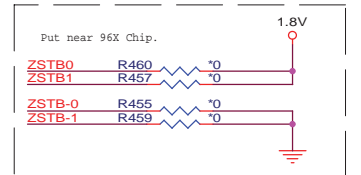
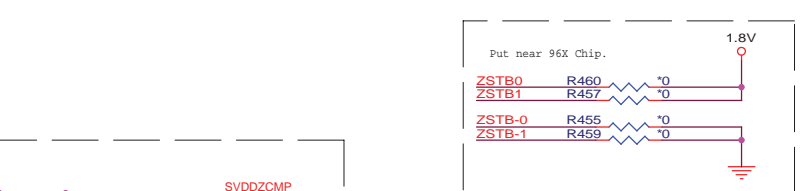
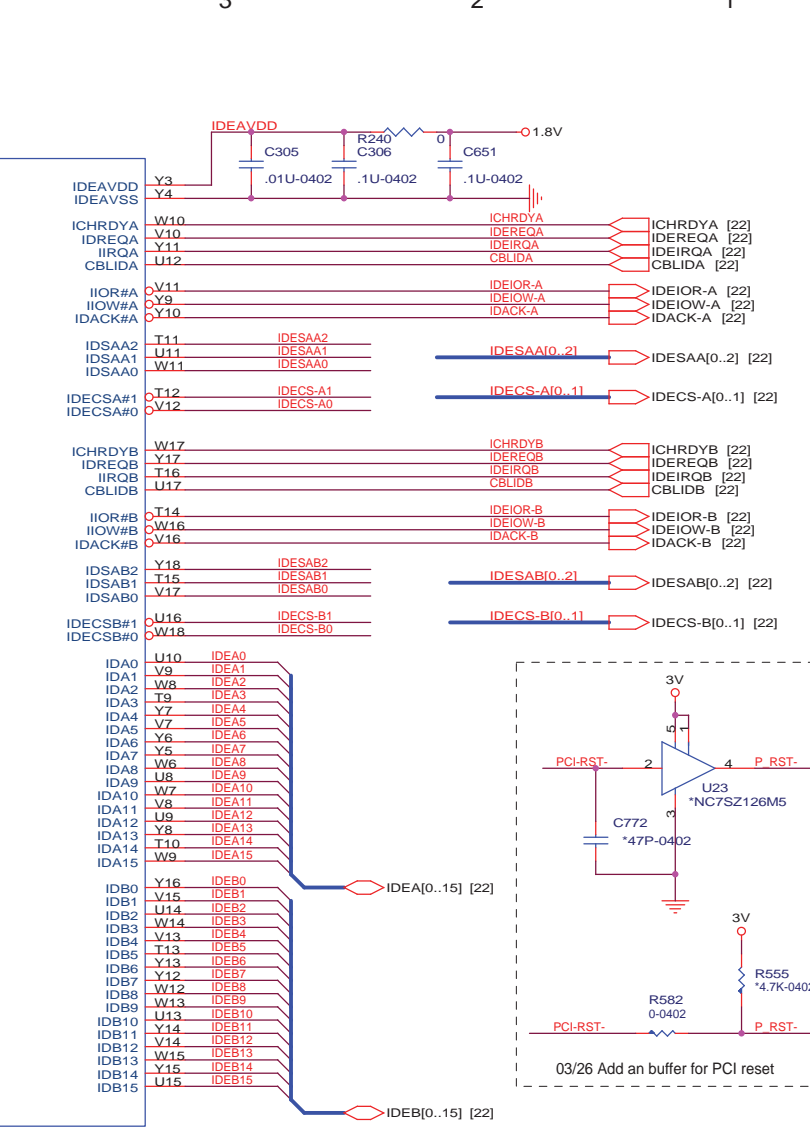
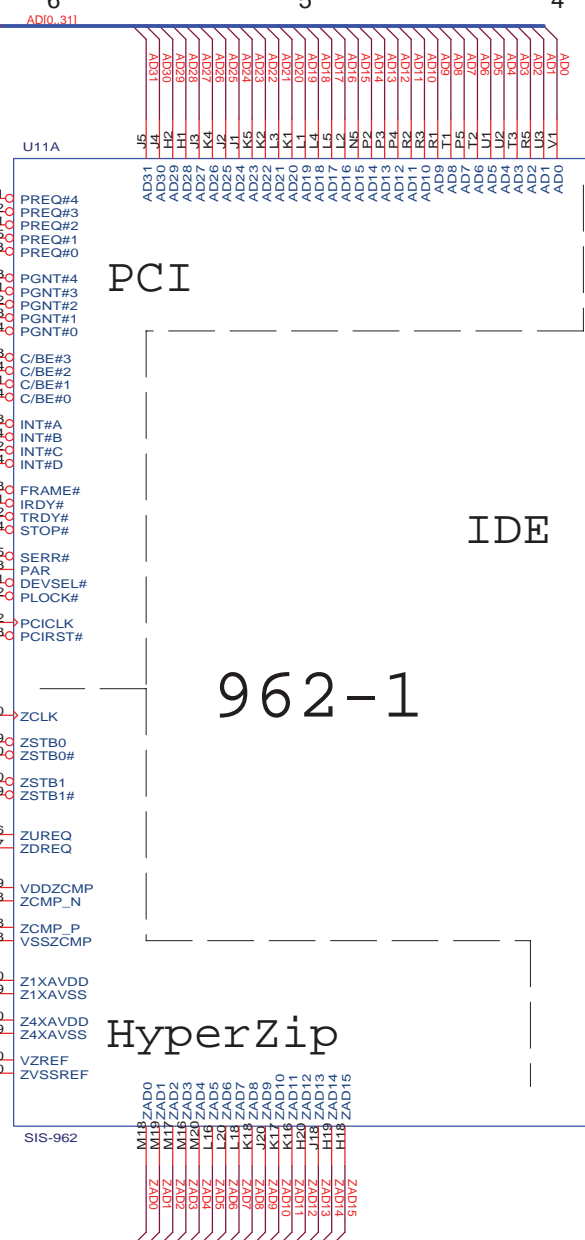
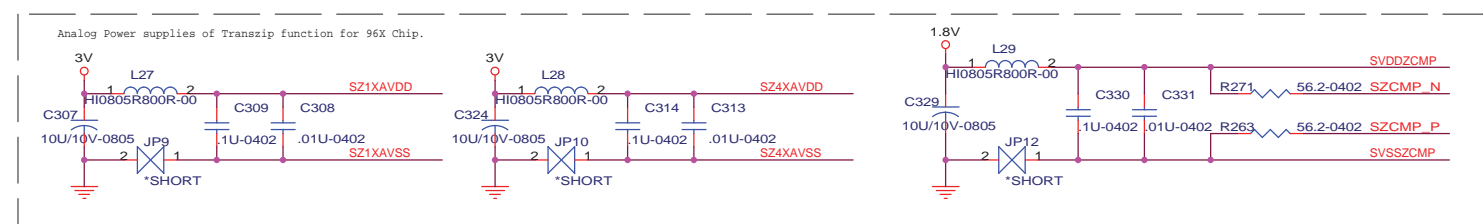
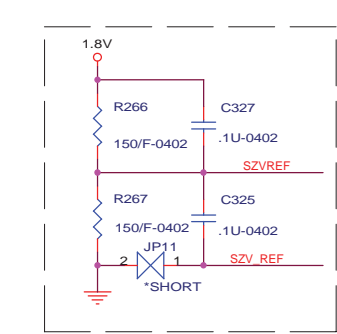
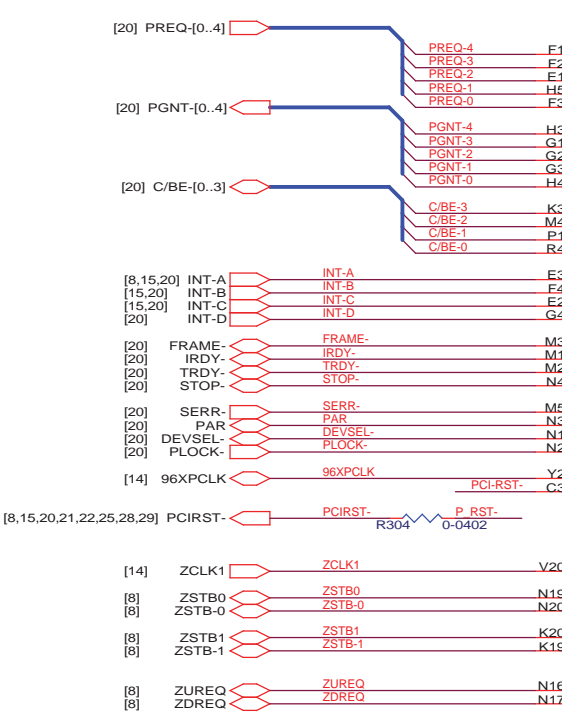
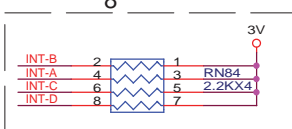
*TPTP11



PROJECT : DT1
Quanta Computer Inc.

Size: Custom Document Number: NB1-HyperZip/VGA/Misc. Rev: E
Date: Friday, April 04, 2003 Sheet: 8 of 35

<http://hobi-elektronika.net>

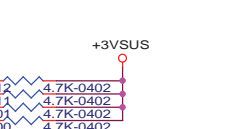
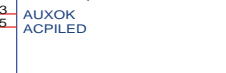
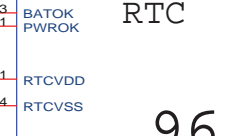
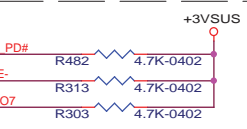
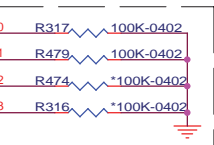
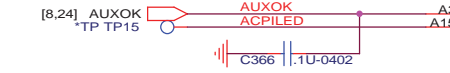
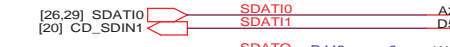
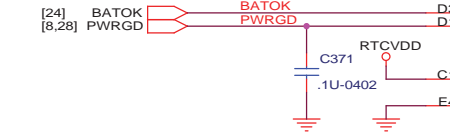
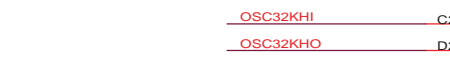
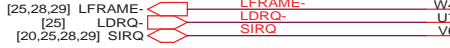
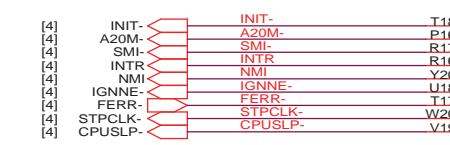


D

C

B

A



APIC

LPC

RTC

962-2

GPIO

AC97

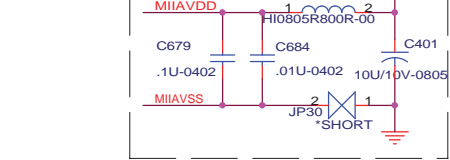
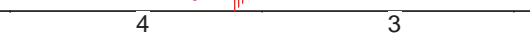
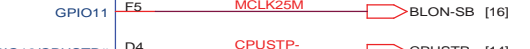
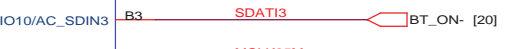
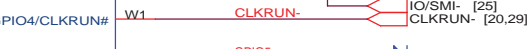
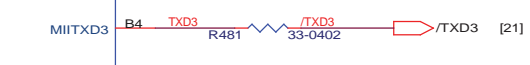
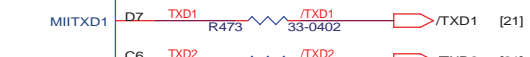
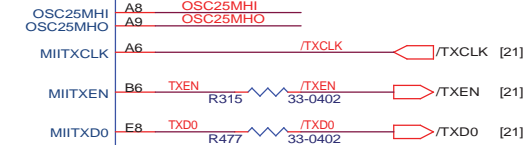
ACPI
/others

KBC
/geyserville

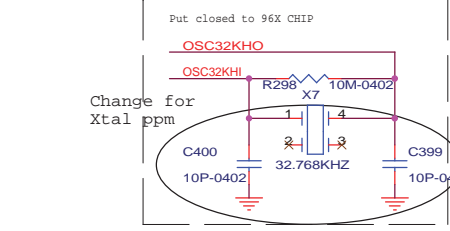
SIS-962

MII

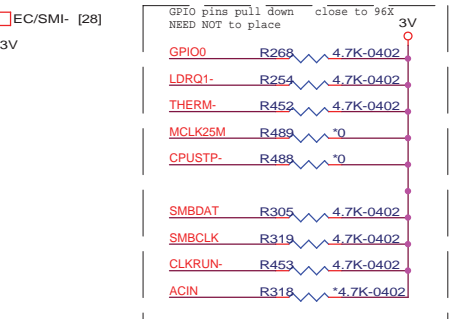
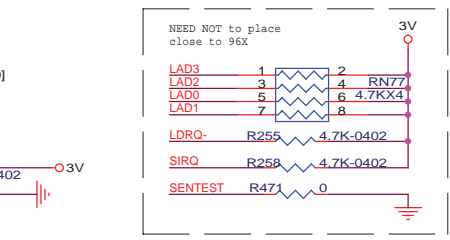
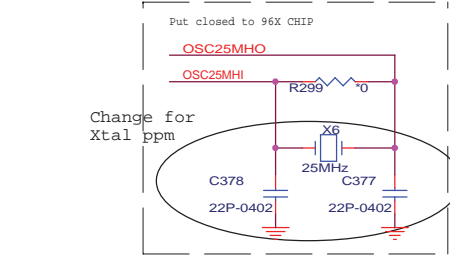
GPIO



02/28 X7 COMPONENT FROM BG332768721 TO BG33768216

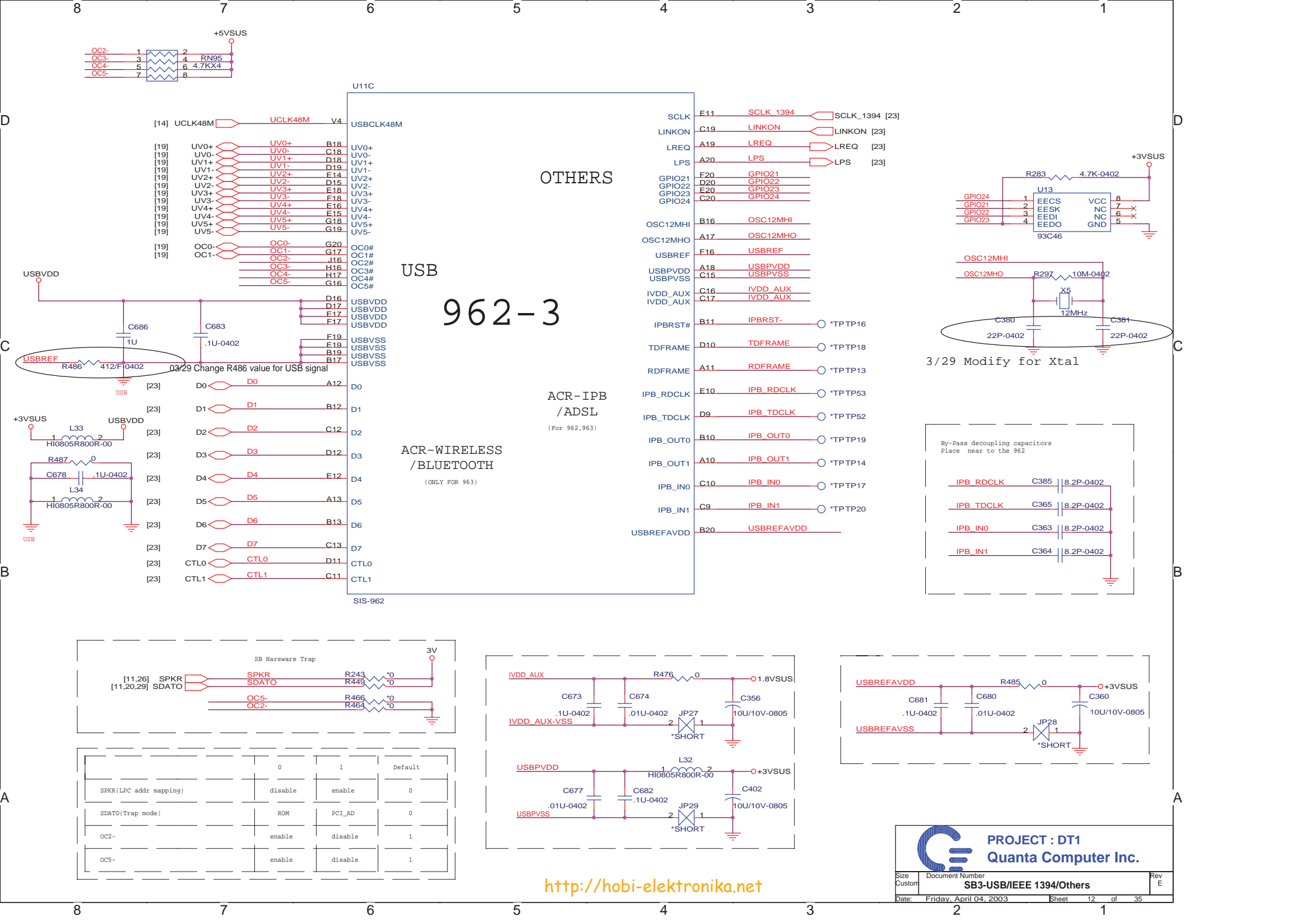


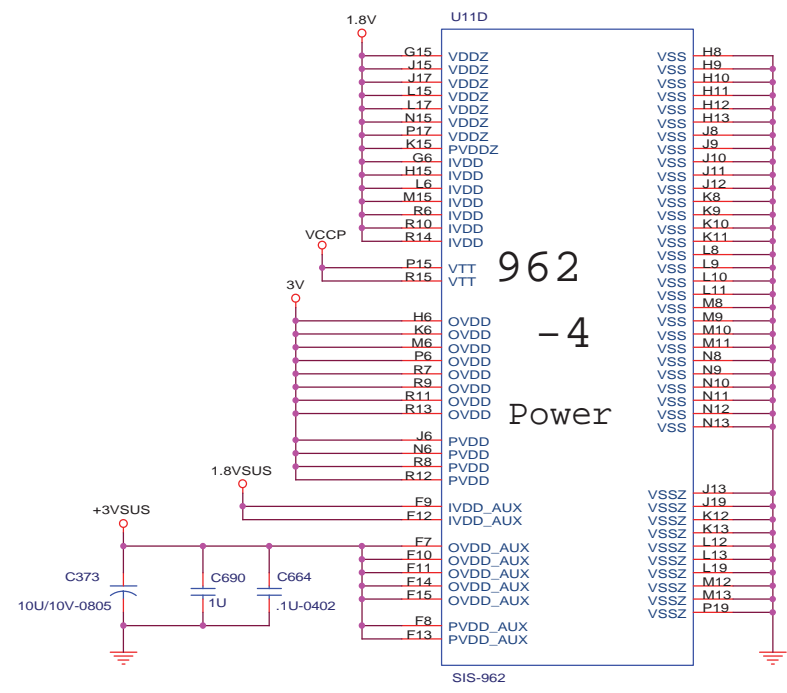
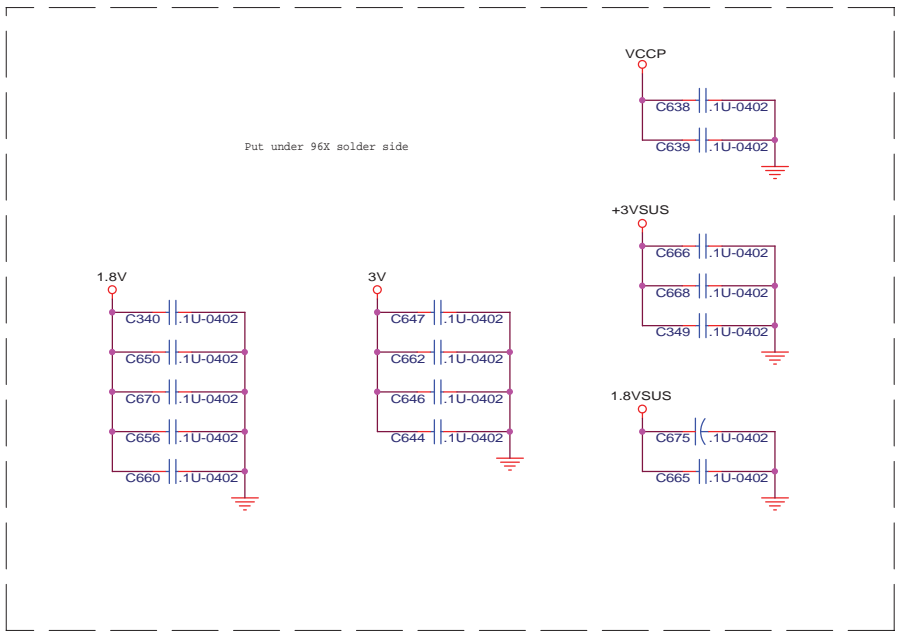
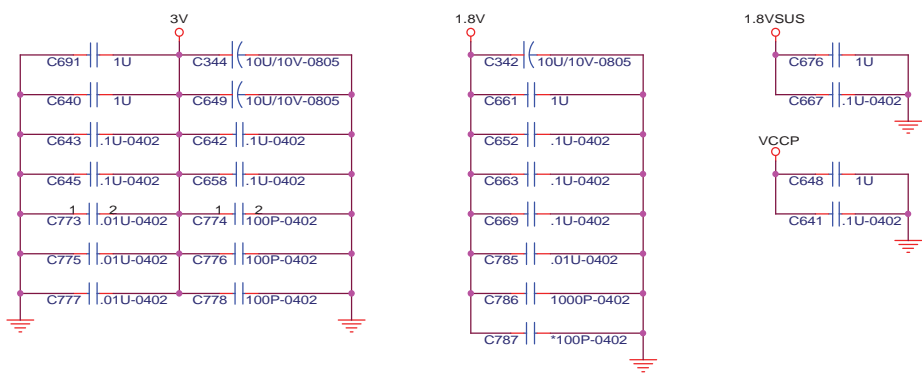
02/28 C399 FROM 20P TO 10P, C400 FROM 15P TO 10P



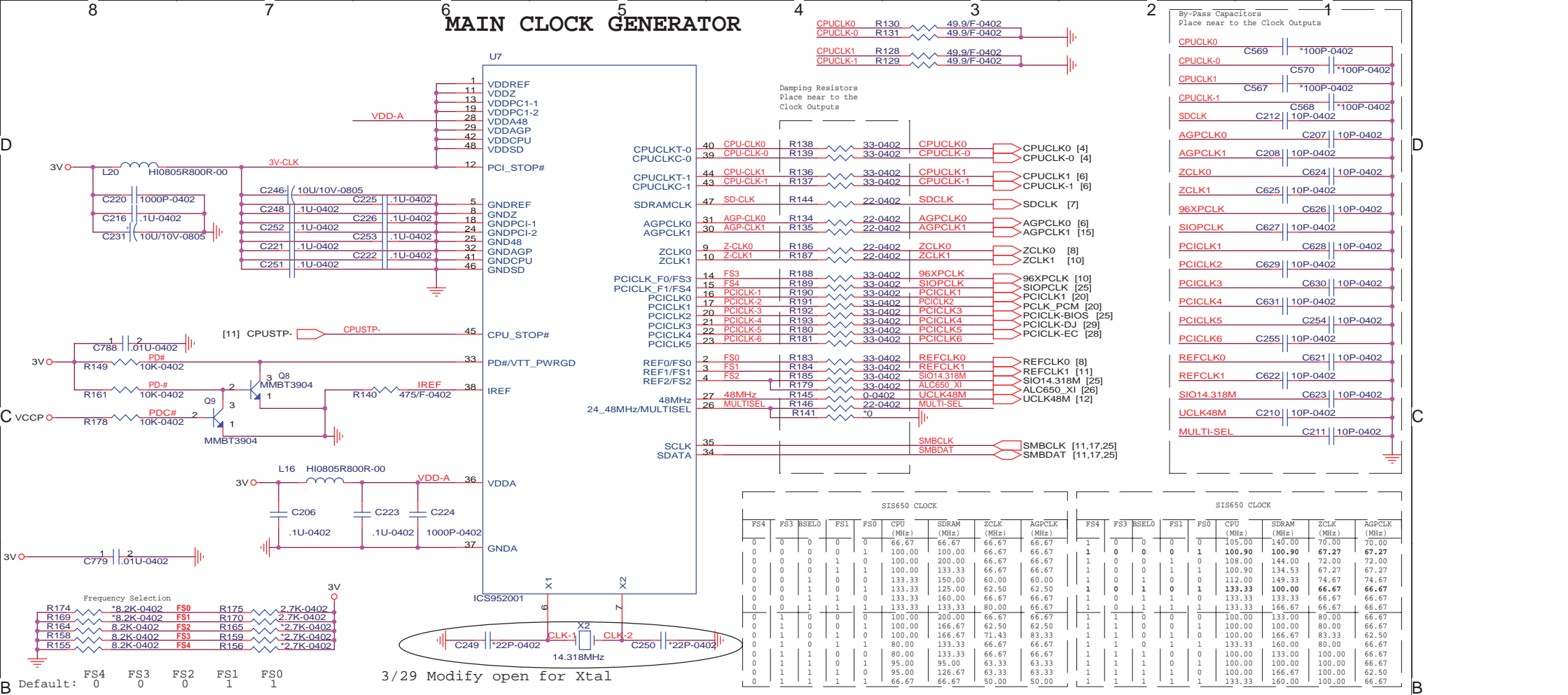
PROJECT : DT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB2-Misc Signals	E
Date:	Friday, April 04, 2003	Sheet 11 of 35

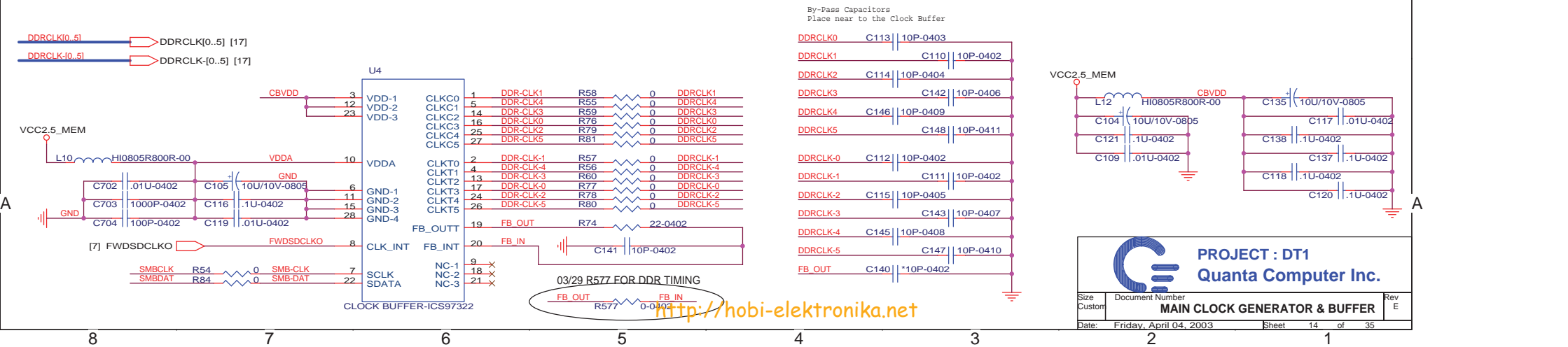




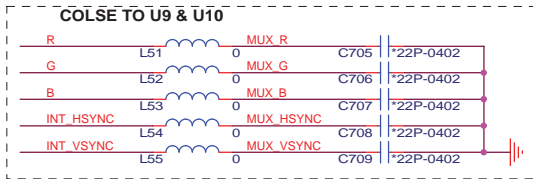
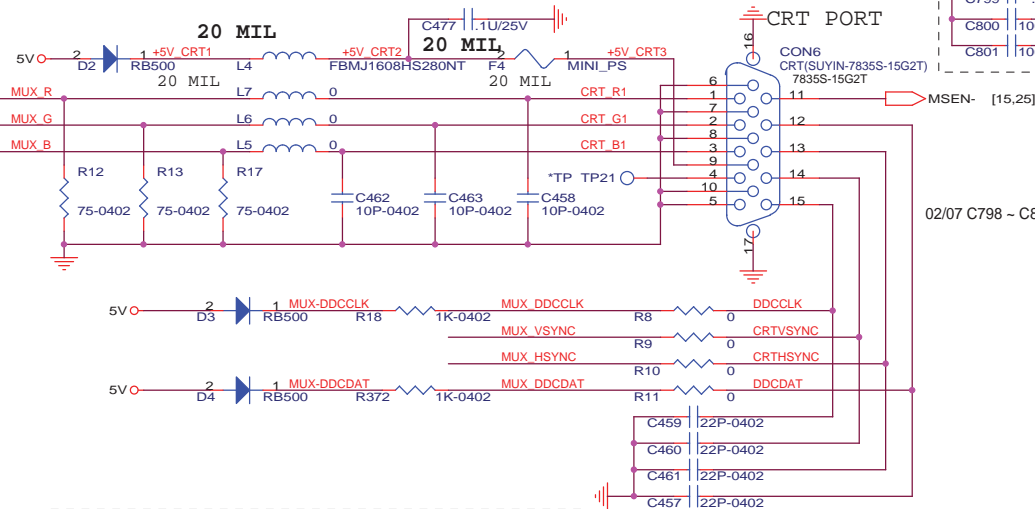
MAIN CLOCK GENERATOR



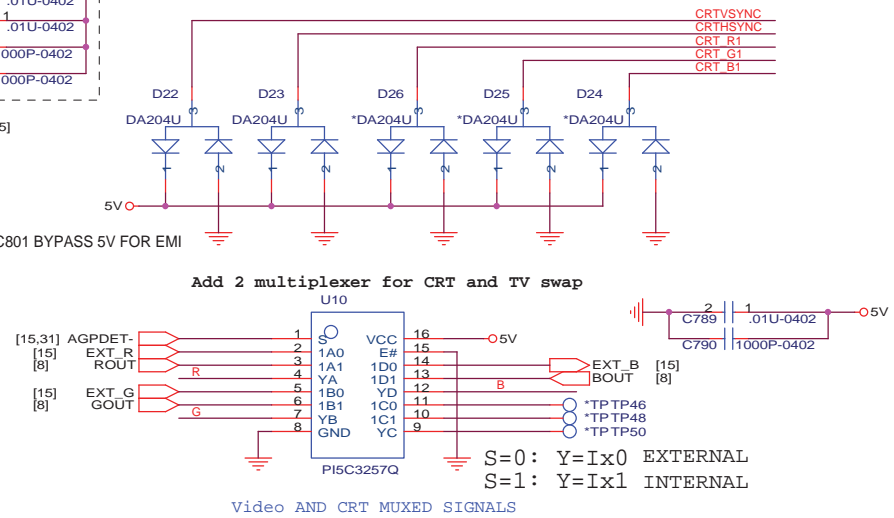
CLOCK BUFFER



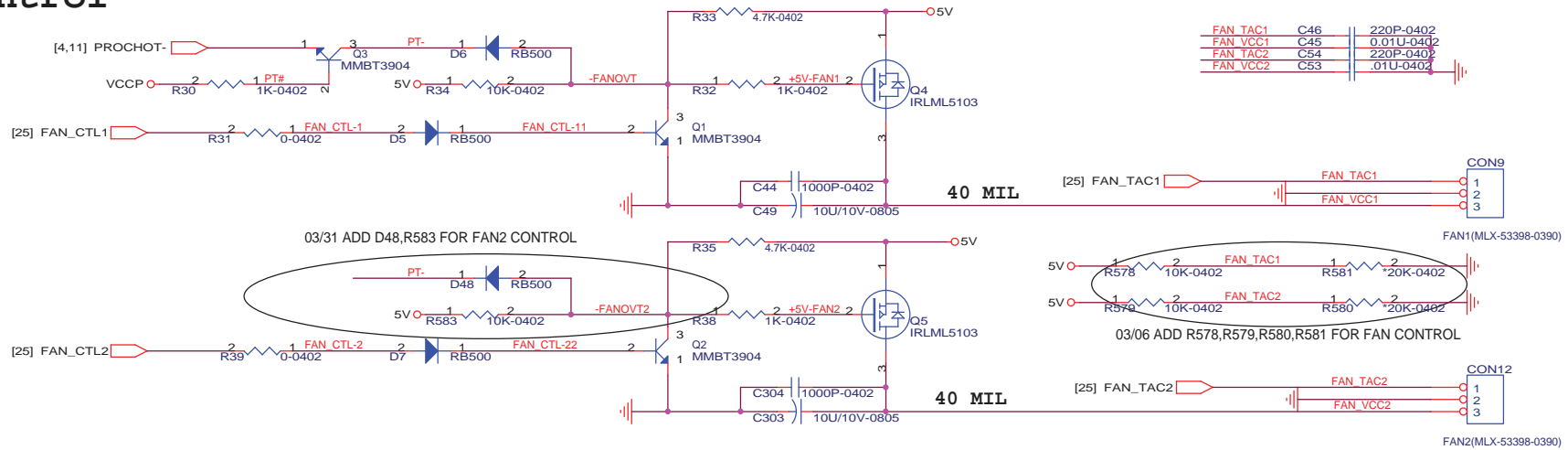
CRT



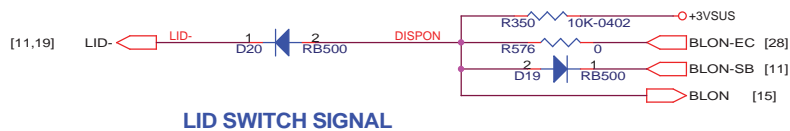
PSOT05LC



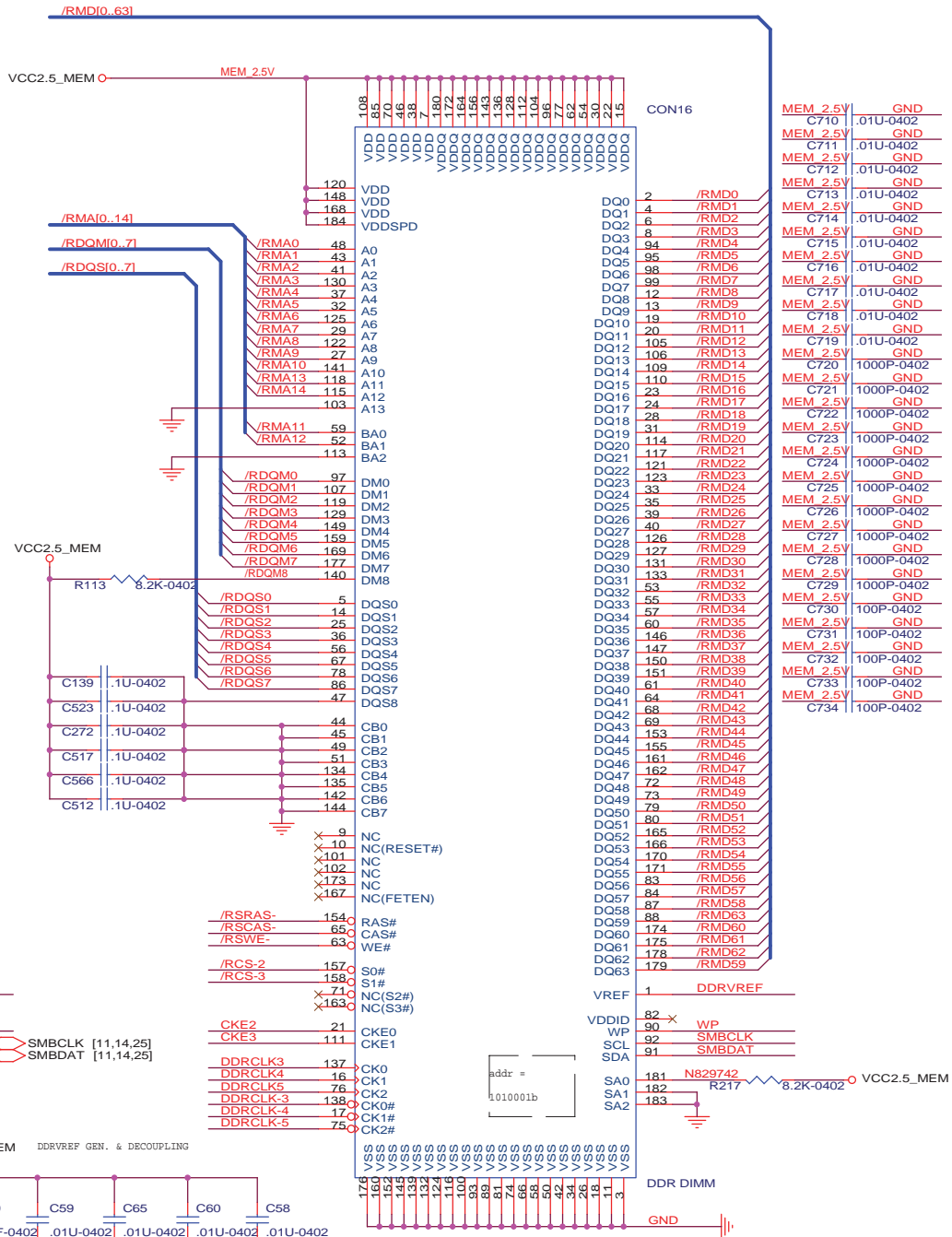
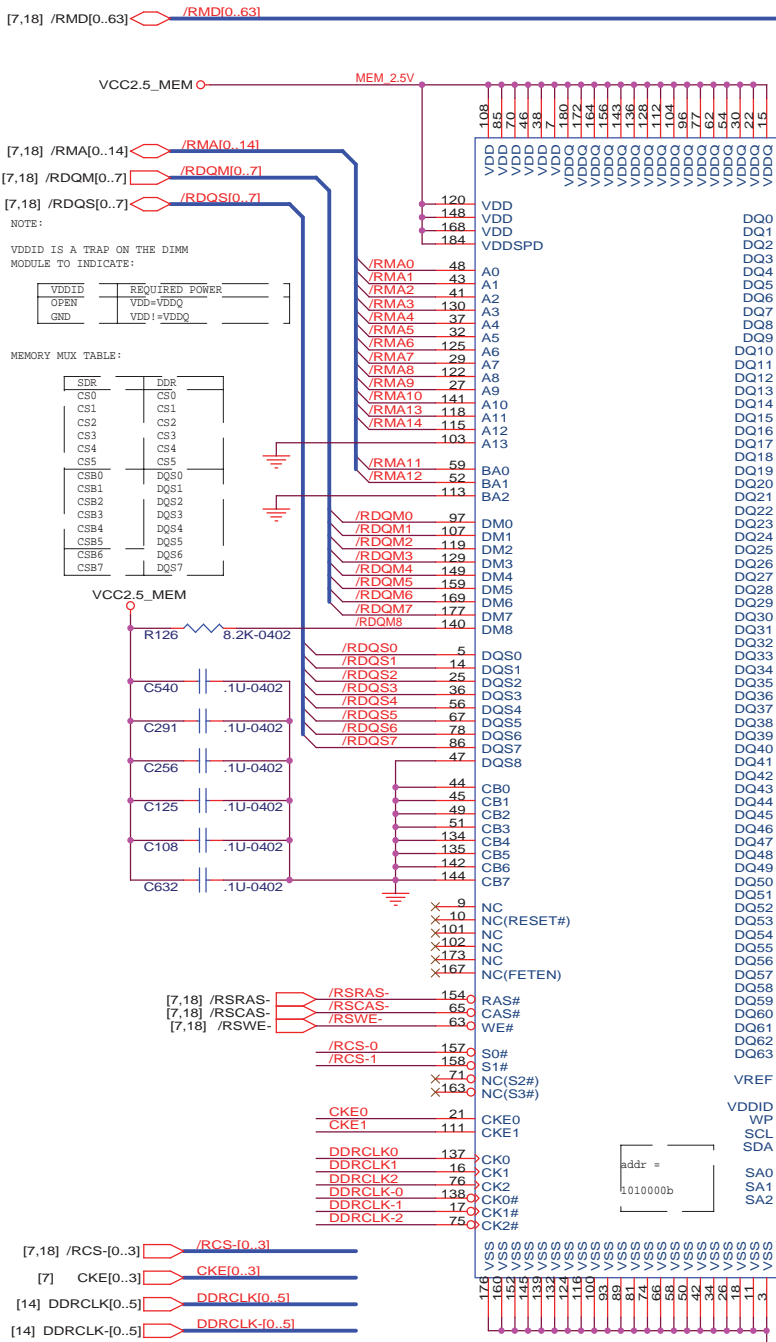
FAN Control



LCD-LID



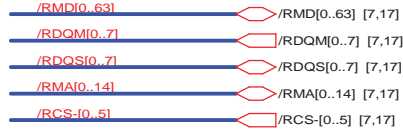
PROJECT : DT1
Quanta Computer Inc.



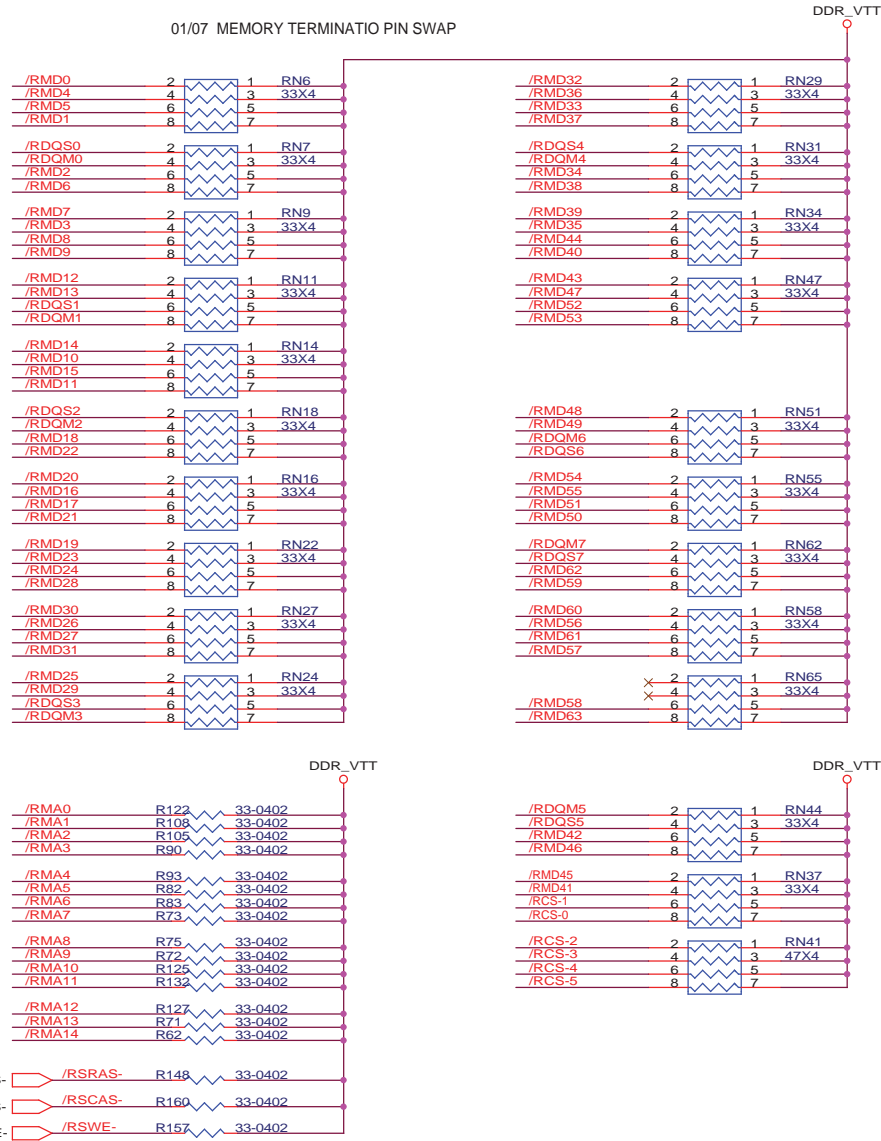
MEM 2.5V	GND
C710	.01U-0402
MEM 2.5V	GND
C711	.01U-0402
MEM 2.5V	GND
C712	.01U-0402
MEM 2.5V	GND
C713	.01U-0402
MEM 2.5V	GND
C714	.01U-0402
MEM 2.5V	GND
C715	.01U-0402
MEM 2.5V	GND
C716	.01U-0402
MEM 2.5V	GND
C717	.01U-0402
MEM 2.5V	GND
C718	.01U-0402
MEM 2.5V	GND
C719	.01U-0402
MEM 2.5V	GND
C720	1000P-0402
MEM 2.5V	GND
C721	1000P-0402
MEM 2.5V	GND
C722	1000P-0402
MEM 2.5V	GND
C723	1000P-0402
MEM 2.5V	GND
C724	1000P-0402
MEM 2.5V	GND
C725	1000P-0402
MEM 2.5V	GND
C726	1000P-0402
MEM 2.5V	GND
C727	1000P-0402
MEM 2.5V	GND
C728	1000P-0402
MEM 2.5V	GND
C729	1000P-0402
MEM 2.5V	GND
C730	100P-0402
MEM 2.5V	GND
C731	100P-0402
MEM 2.5V	GND
C732	100P-0402
MEM 2.5V	GND
C733	100P-0402
MEM 2.5V	GND
C734	100P-0402

SSTL-2 Termination Resistors

	SDR		DDR		
MD/DQM(/DQS)	LV-CMOS	R _s 0/10/-	SSTL-2	R _s 10	R _{tt} 33
MA/Control	LV-CMOS	10	SSTL-2	0	33
CSE	OD 3.3V	0	SSTL-2	0	47
			OD 2.5V		

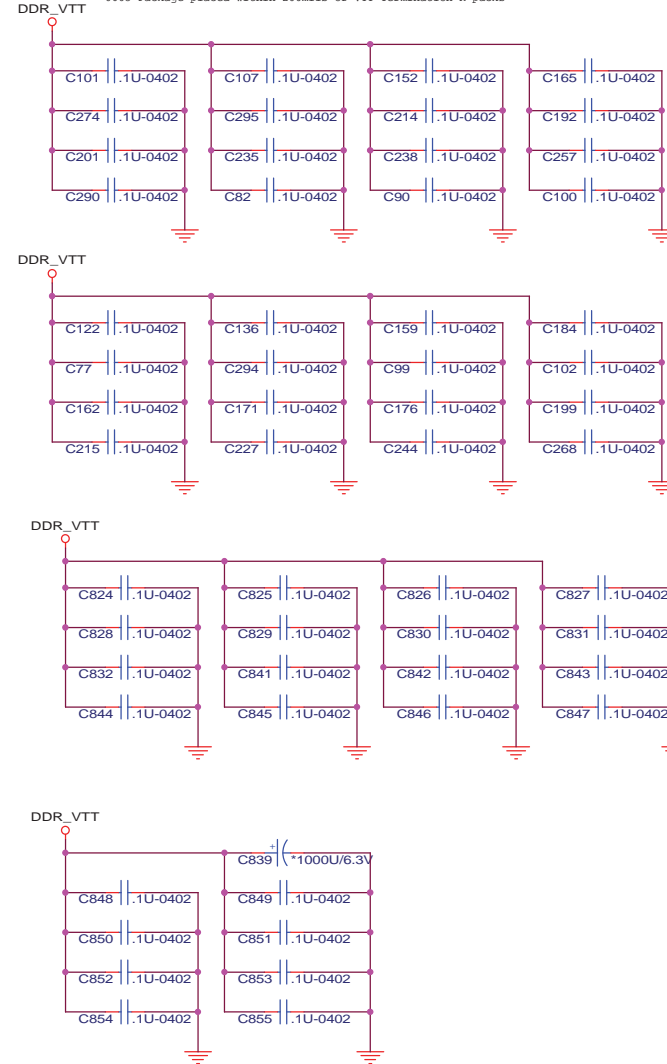


01/07 MEMORY TERMINATIO PIN SWAP



DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND

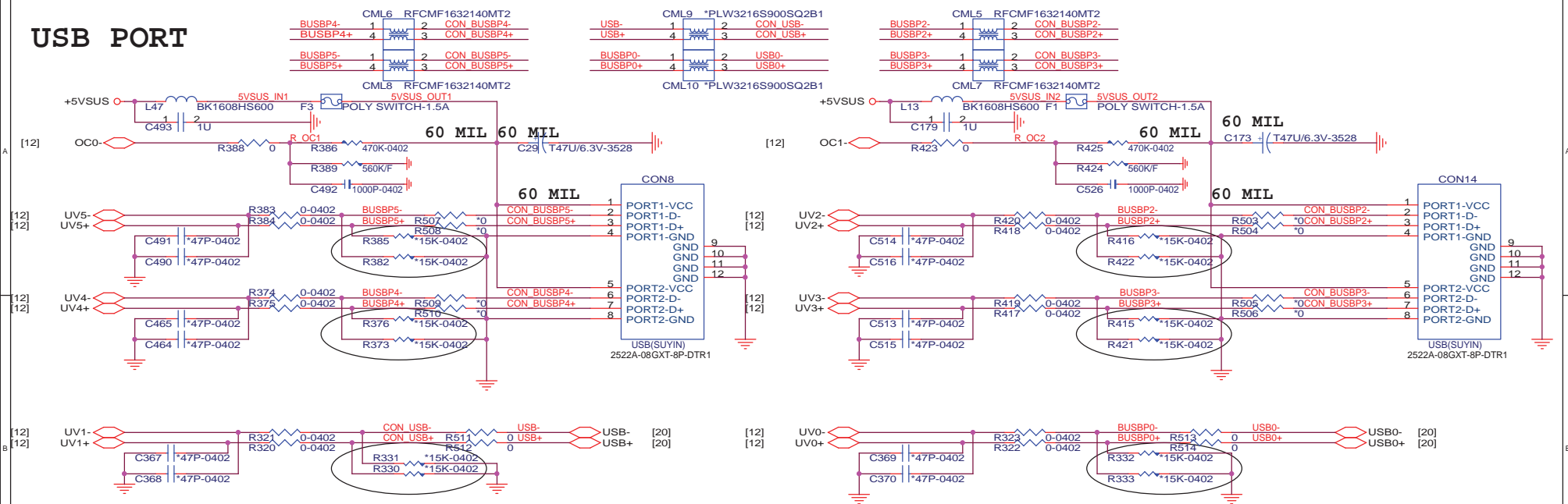
0603 Package placed within 200mils of VTT Termination R-packs



PROJECT : DT1
Quanta Computer Inc.

Size Custom	Document Number SSTL-2 TERMINATION RESISTORS	Rev E
Date: Friday, April 04, 2003	Sheet 18 of 35	

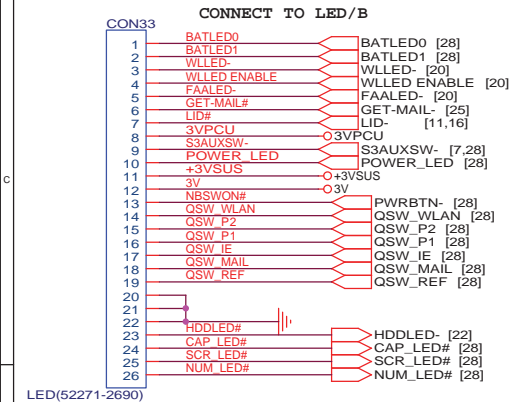
USB PORT



LED/B CONNECTOR

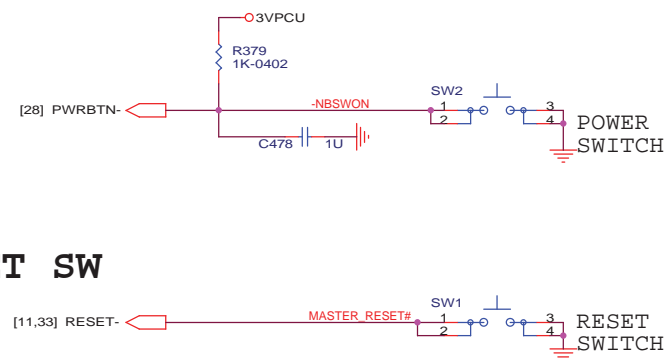
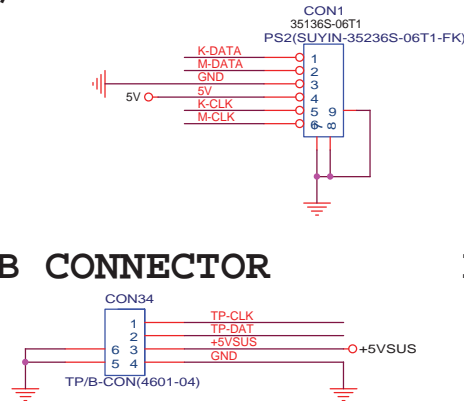
PS/2

POWER SW



TP/B CONNECTOR

RESET SW



QSW P1	C262	*1U-0402	C452	*1U-0402	3V
QSW P2	C266	*1U-0402	C482	*1U-0402	+5VSUS
NBSWON#	C233	220P-0402	C269	*1U-0402	3VPCU
WLED ENABLE	C233	220P-0402	C269	*1U-0402	QSW_REF
QSW WLAN	C247	220P-0402	C228	*1U-0402	BATLED0
QSW MAIL	C258	*1U-0402	C230	*1U-0402	BATLED1
QSW IE	C260	*1U-0402	C232	220P-0402	WLED-
HDDLED#	C273	220P-0402	C239	220P-0402	GET-MAIL#
CAP_LED#	C275	220P-0402	C242	*47P-0402	TP-DAT
SCR_LED#	C280	220P-0402	C243	*47P-0402	TP-CLK
NUM_LED#	C281	220P-0402	C240	220P-0402	LIB#

03/06 C241,C241 47P UNSTAFF

02/28 C45,C455,C456,C457 FROM 100P CHANGE TO 270P FOR EMI

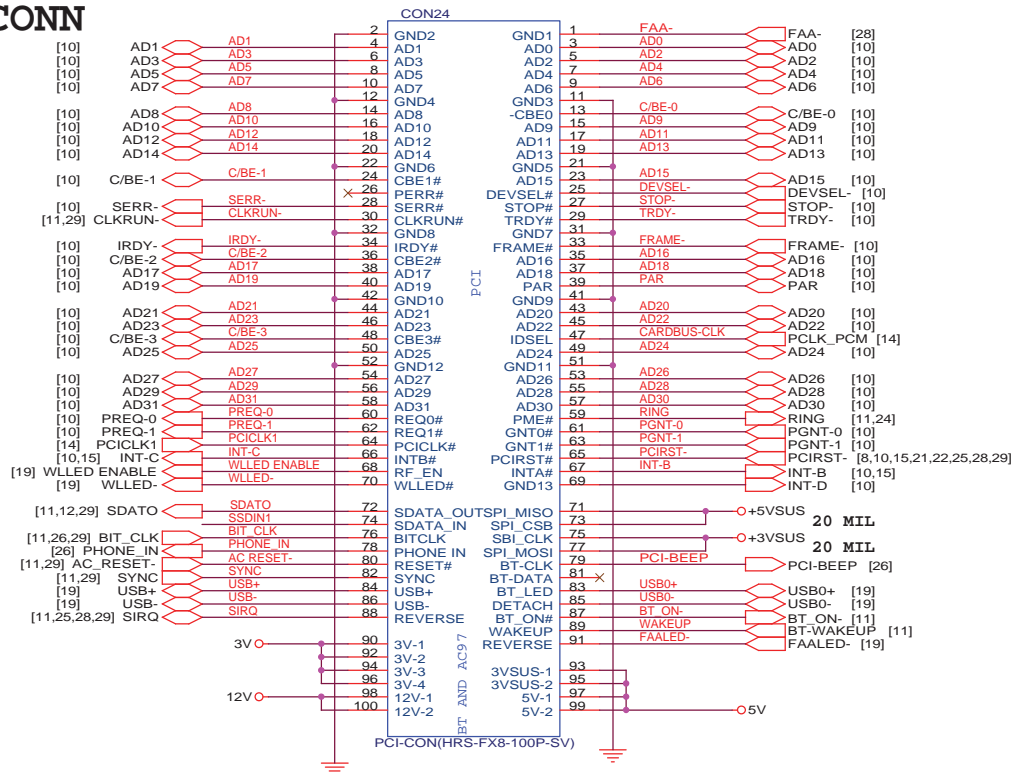


03/06 C453,C454,C455,C456 UNSTAFF

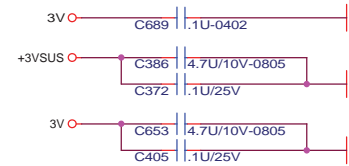
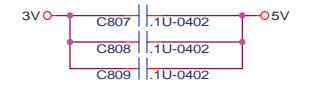
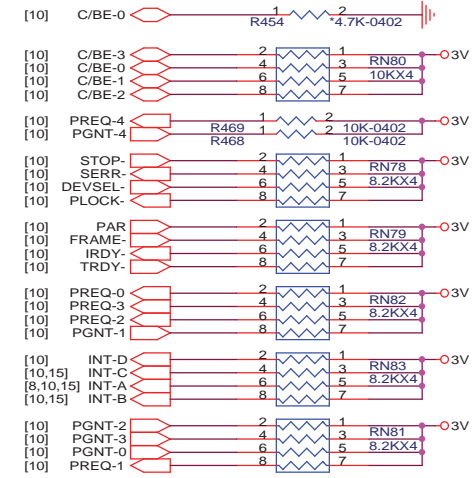
PROJECT : DT1
Quanta Computer Inc.

Size: Custom Document Number: **USB,LED/B,PS2,PW & RST CONN** Rev: E
Date: Friday, April 04, 2003 Sheet: 19 of 35

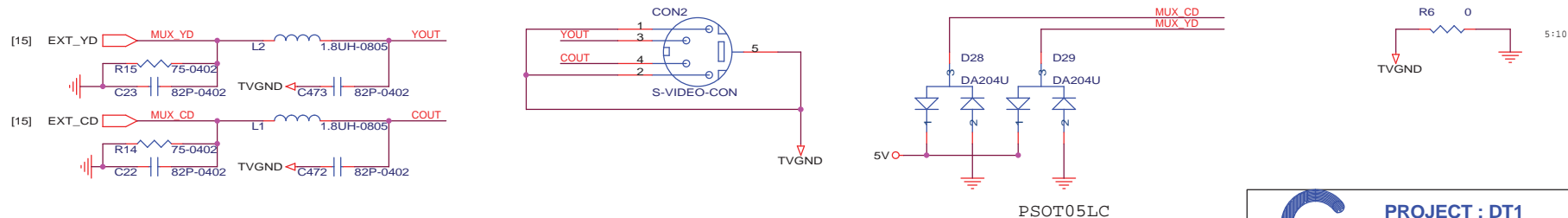
PCI-CONN

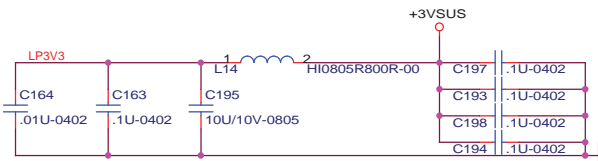
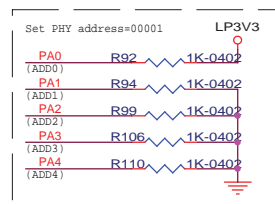
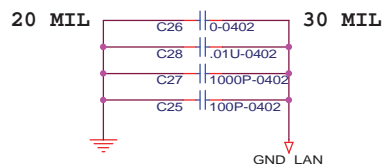
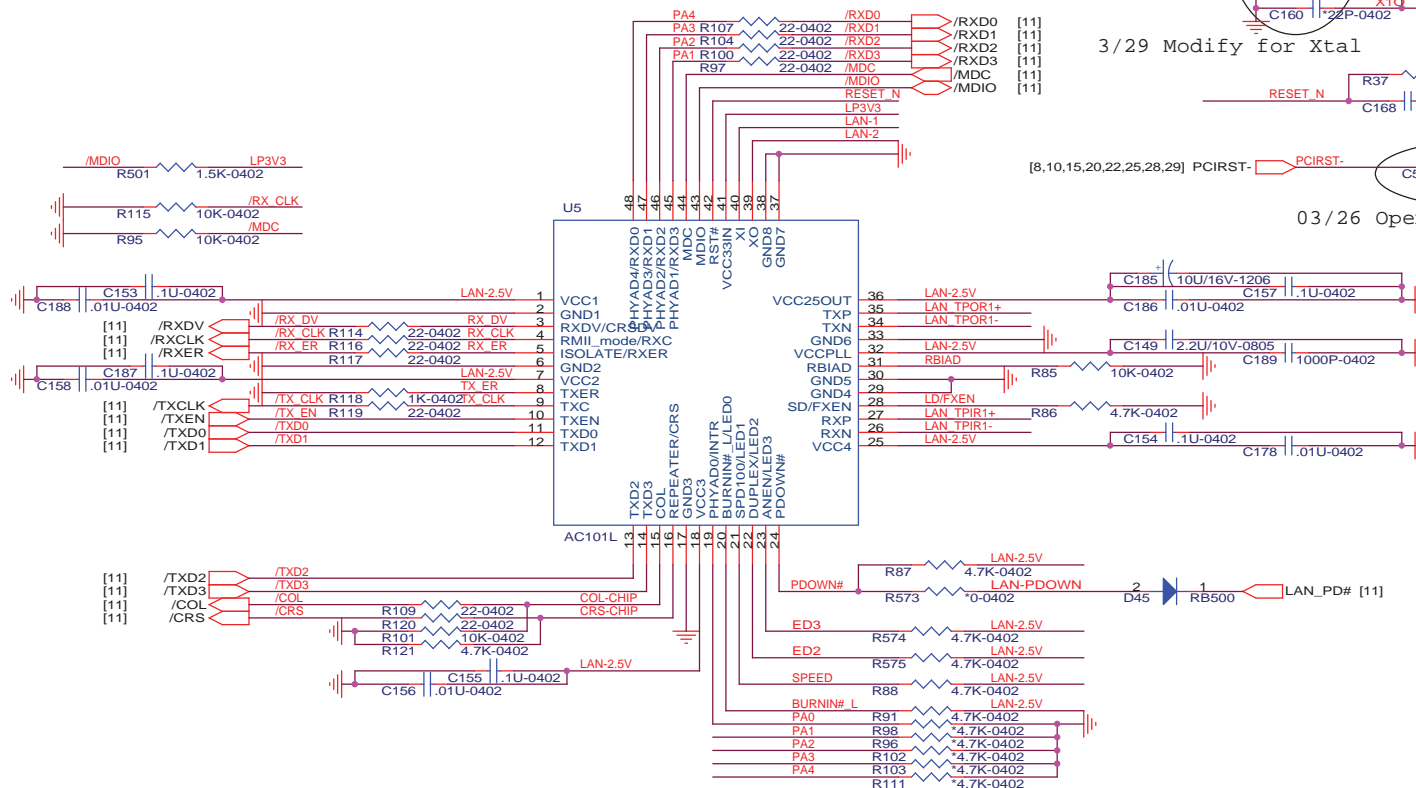
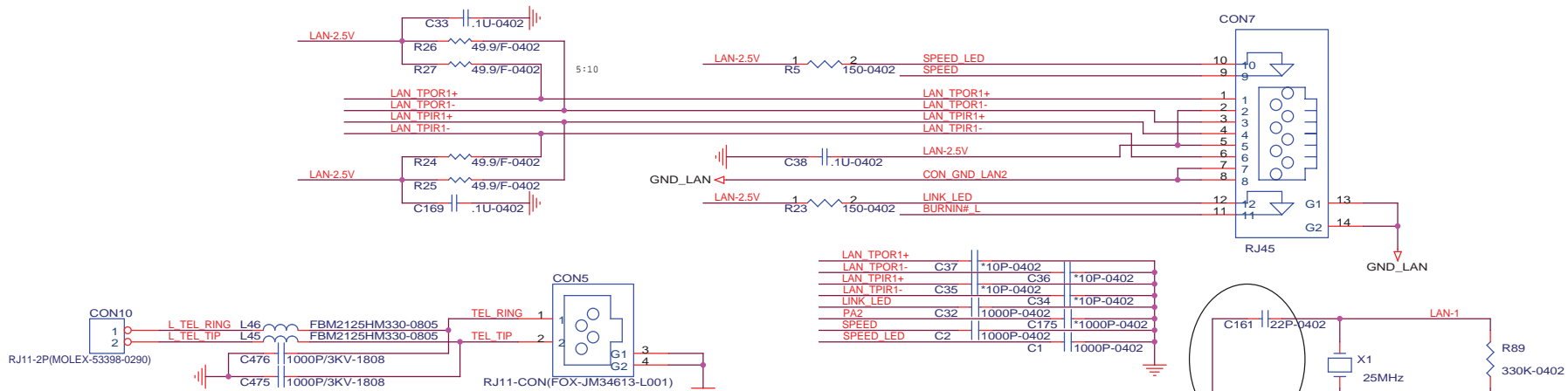


PCI PULL UP



S-VIDEO (TV OUT)





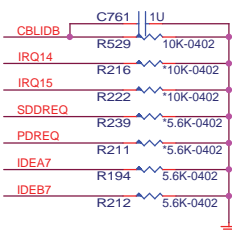
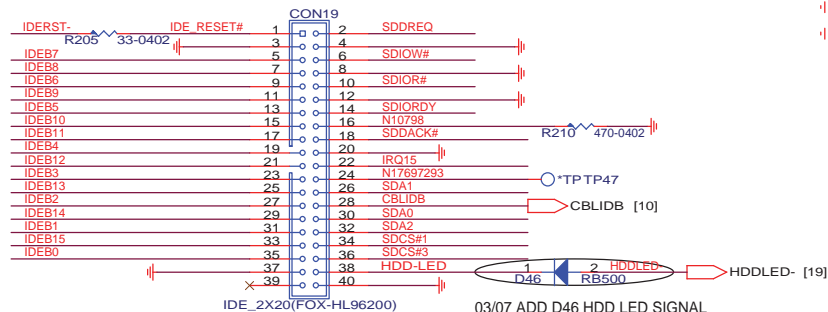
<http://hobi-elektronika.net>

PROJECT : DT1
Quanta Computer Inc.

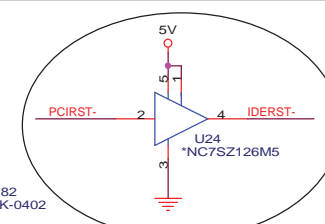
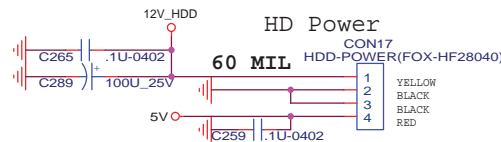
Size: Custom
Document Number: LAN PHY (AC101L) & RJ45,RJ11
Date: Friday, April 04, 2003
Sheet: 21 of 35
Rev: E

HDD,CD-ROM CONNECTOR

12/18 CON19 CHANGE COMPONENT



HDD POWER CONNECTOR

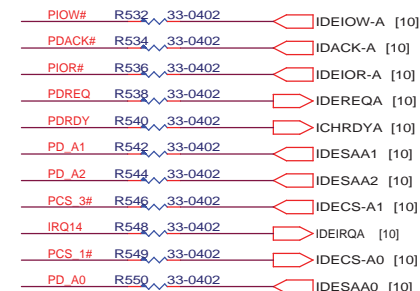


03/26 Add an buffer for IDE reset

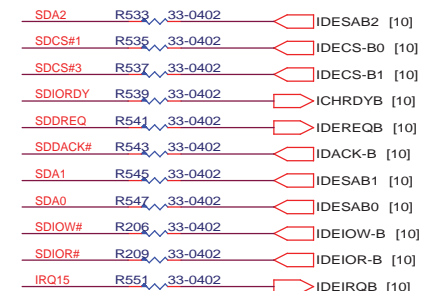


PLACEMENT ON BOT SIDE

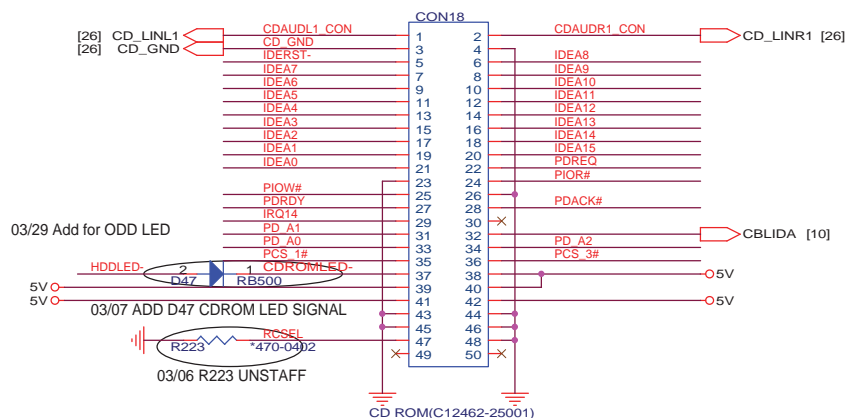
CLOSE TO CHIPSET SIDE



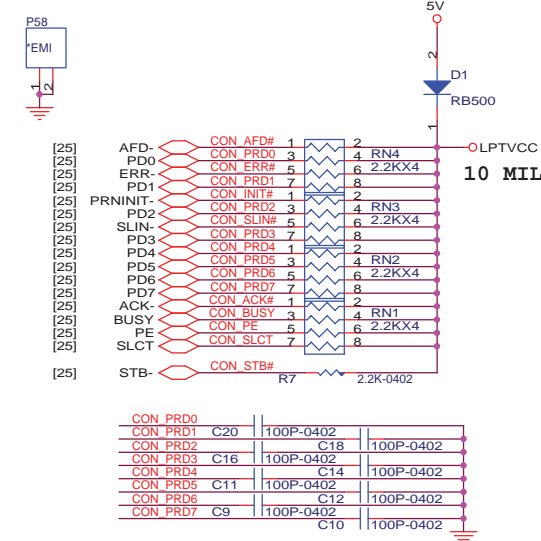
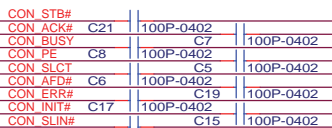
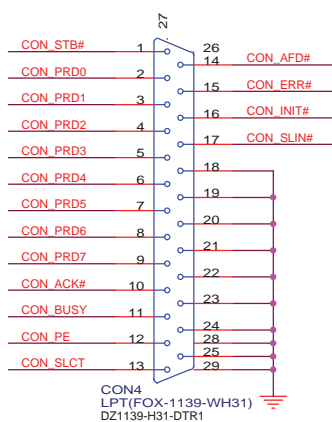
CLOSE TO CHIPSET SIDE



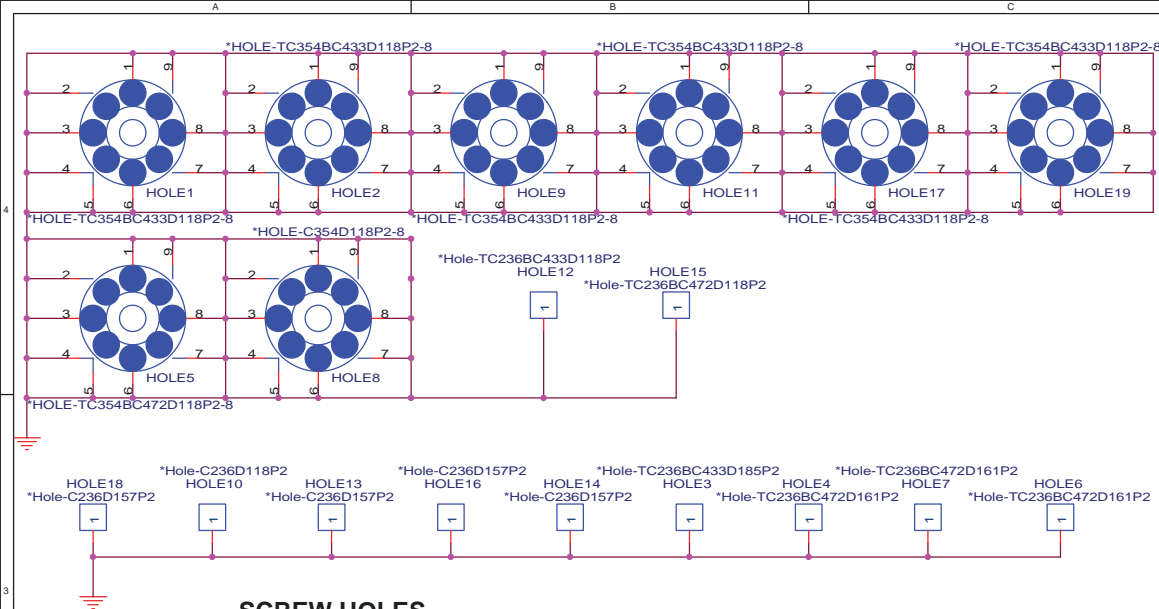
CD-ROM connector



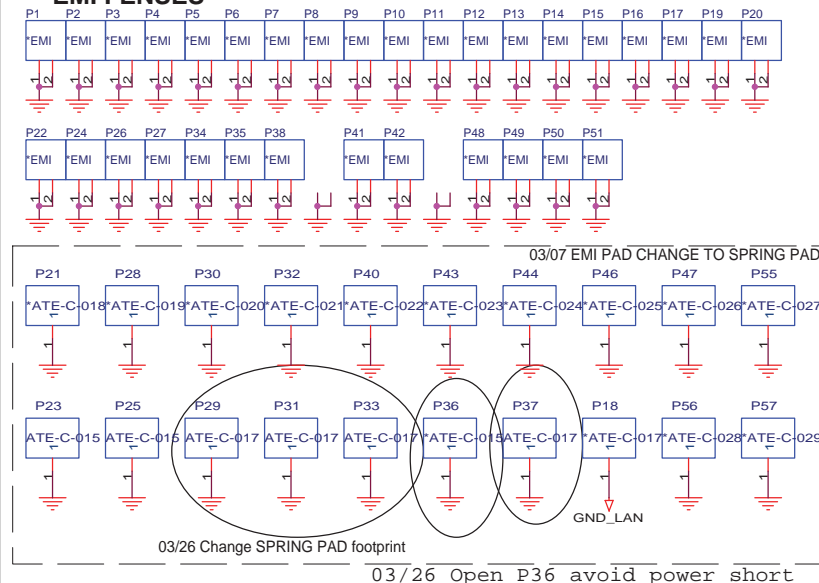
LPT CONN.



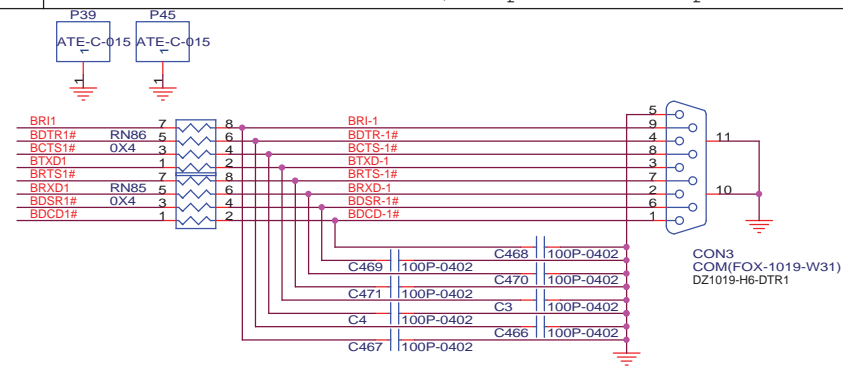
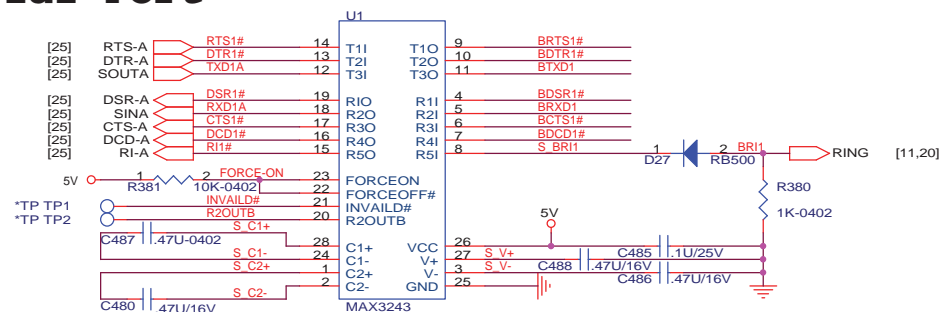
PROJECT : DT1
Quanta Computer Inc.



EMI FENSES



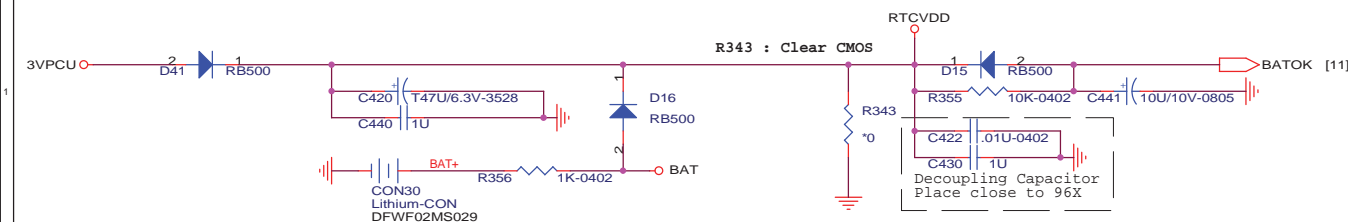
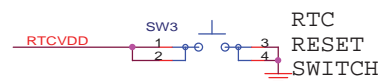
Serial Port



RTC

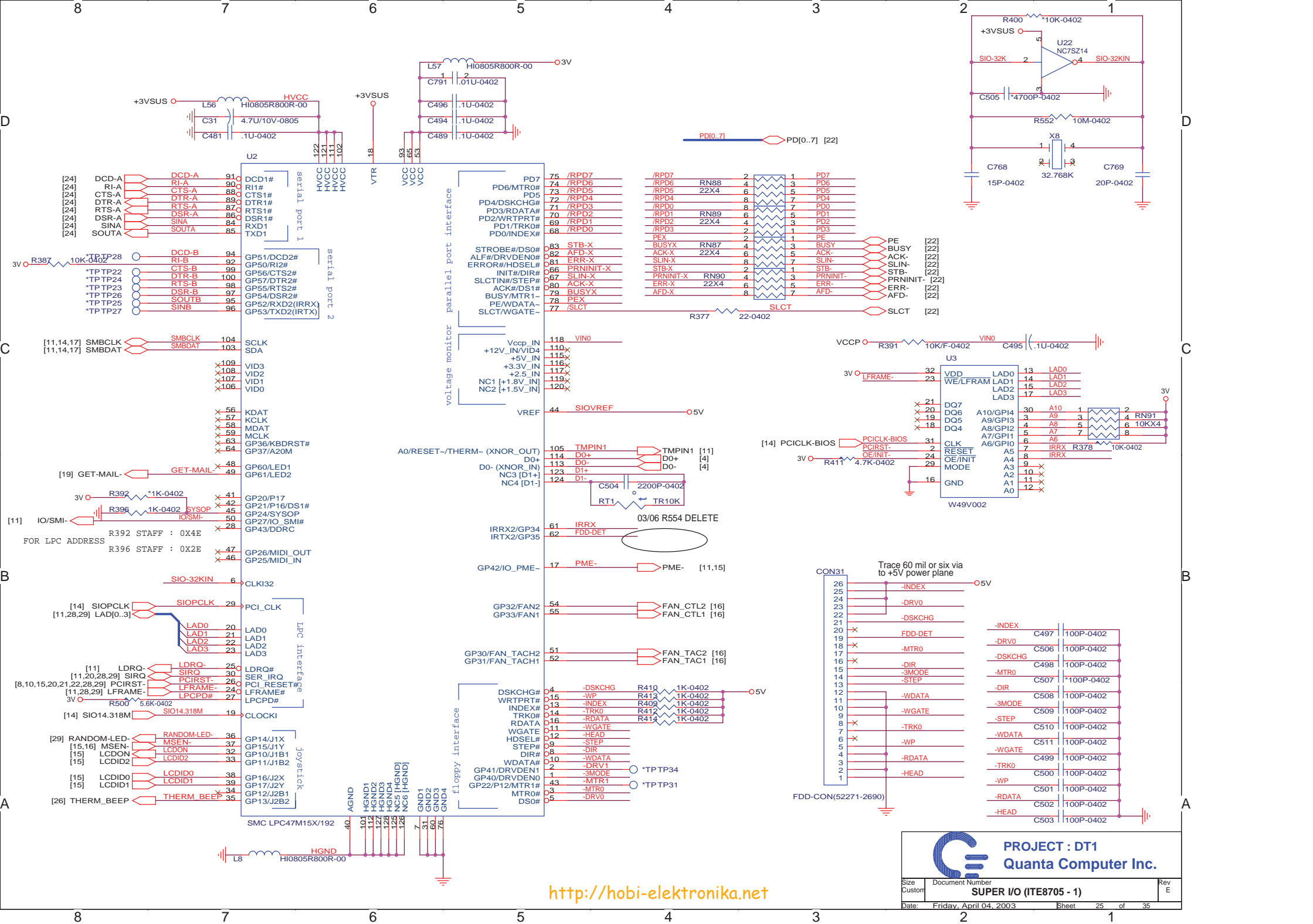
NOTE!

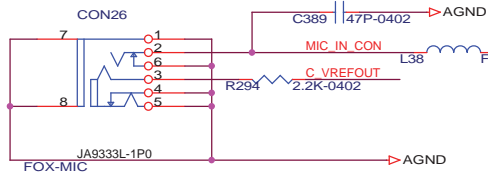
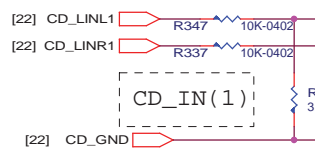
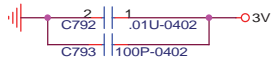
- 1.The RTCVDD is 3V
- 2.Decoupling capacitor must be close to 650 RTCVDD pin.
- 3.RTC circuit must strictly follow SiS's recommended design
SiS is not responsible for RTC problems from foreign designs.



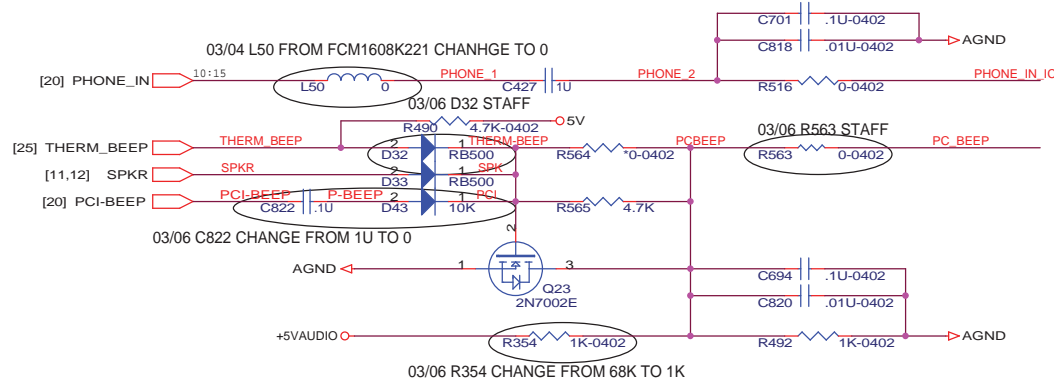
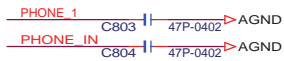
PROJECT : DT1
Quanta Computer Inc.

Size: Custom Document Number: EMI PAD & COM1 Rev: E
Date: Friday, April 04, 2003 Sheet: 24 of 35

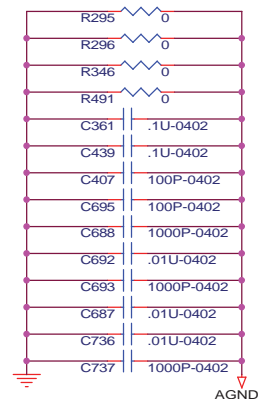
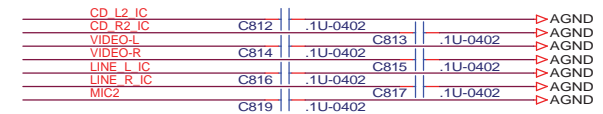
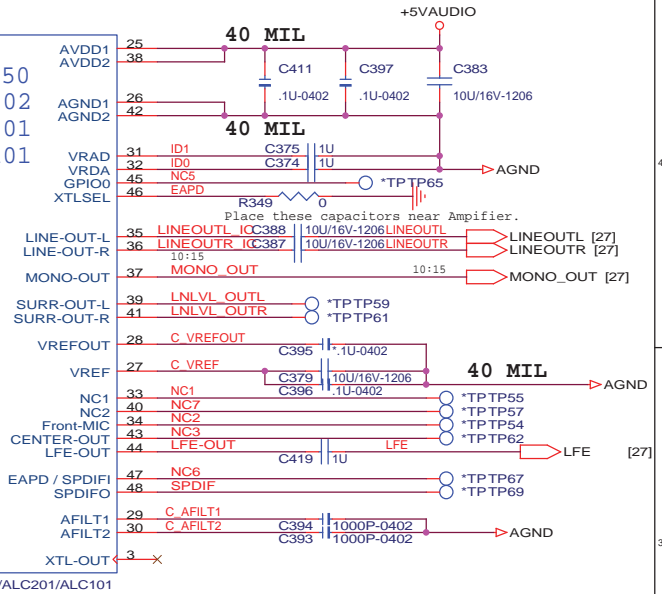
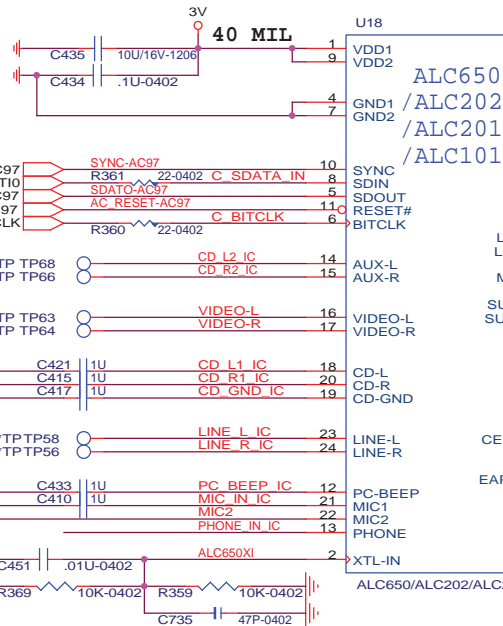
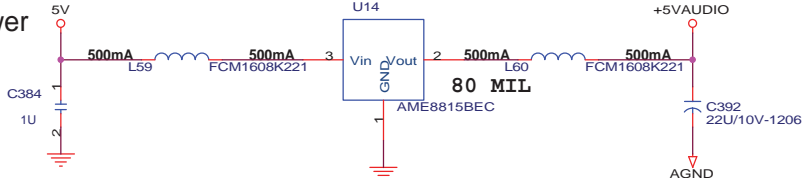




MIC_IN (PINK)

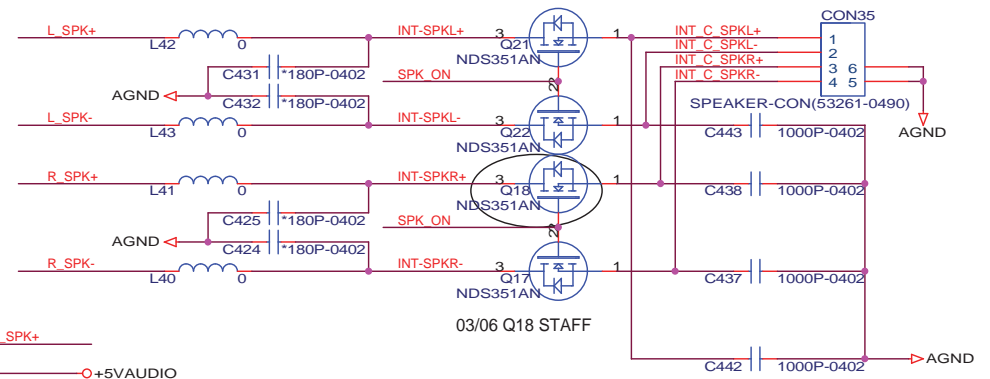
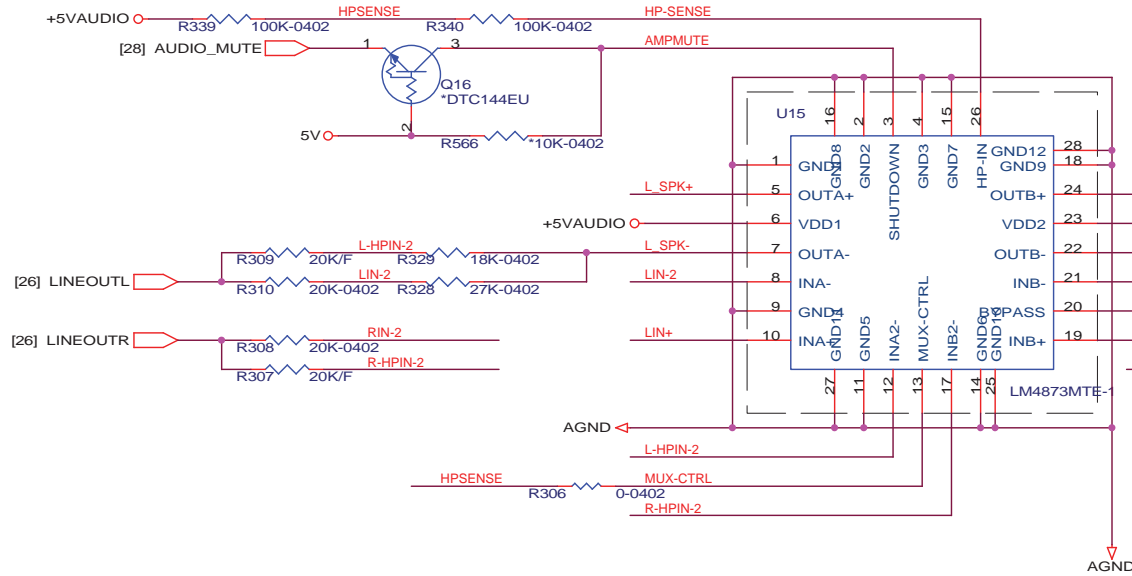


Audio Power

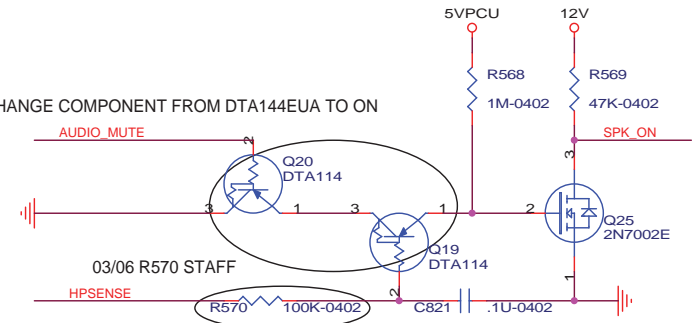


Audio amplifier

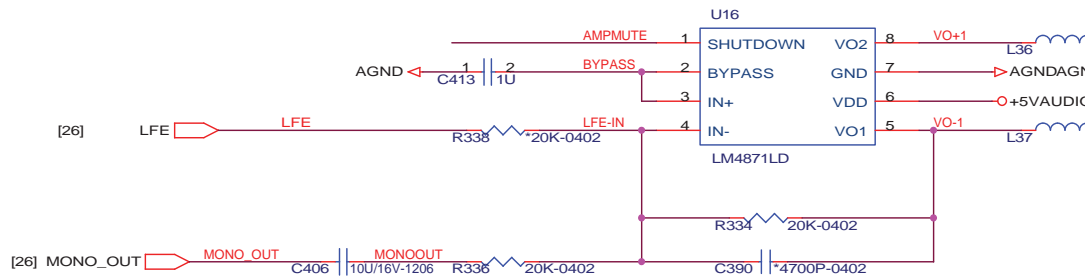
03/06 U15 CHANGE COMPONENT FROM LM4873LQ TO LM4873MTE-1

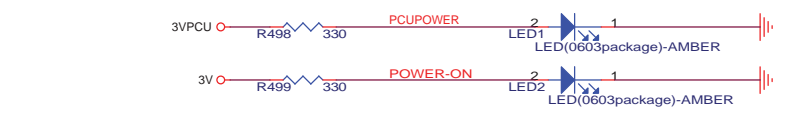
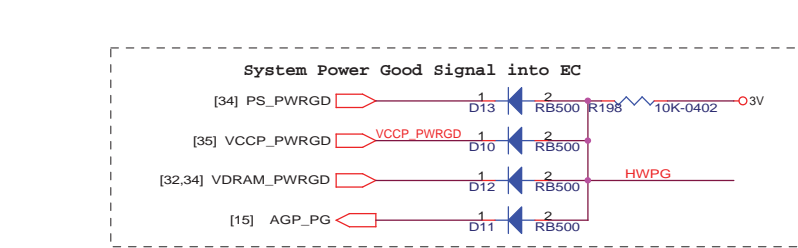
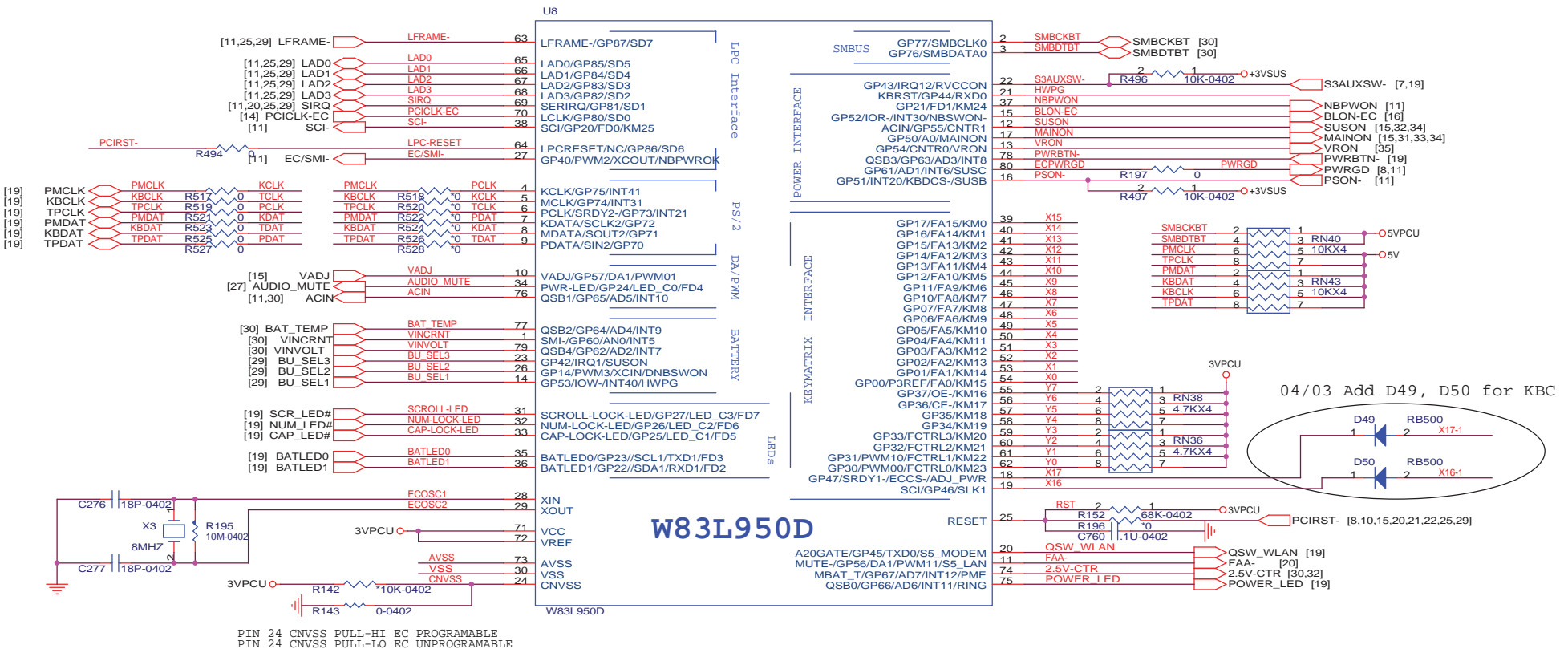


03/06 Q19, Q20 CHANGE COMPONENT FROM DTA144EUA TO ON



03/06 R570 STAFF

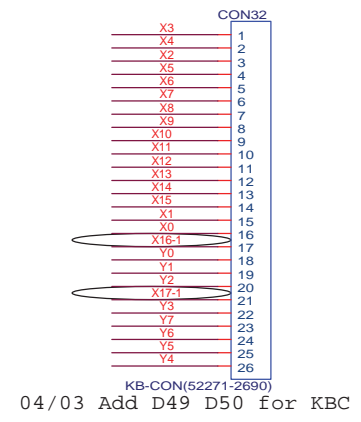





<http://hobi-elektronika.net>

X2 & Y3: E-MAIL
X2 & Y2: EXPLORER
X2 & Y1: P1
X2 & Y0: P2

Y3 QSW_MAIL [19]
Y2 QSW_IE [19]
Y1 QSW_P1 [19]
Y0 QSW_P2 [19]
X2 QSW_REF [19]

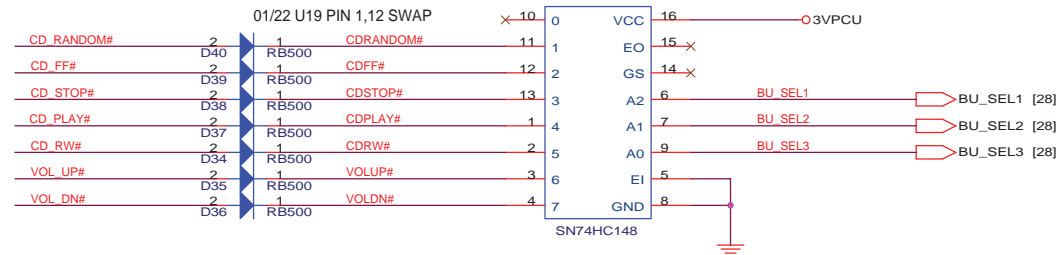
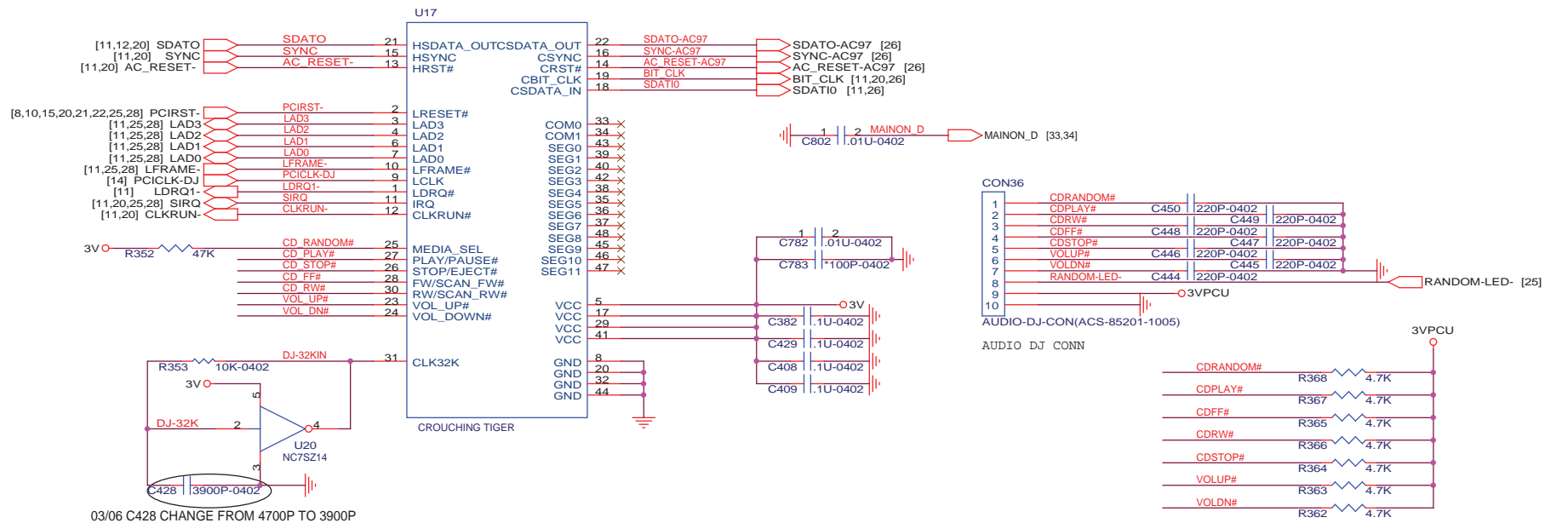


04/03 Add D49 D50 for KBC

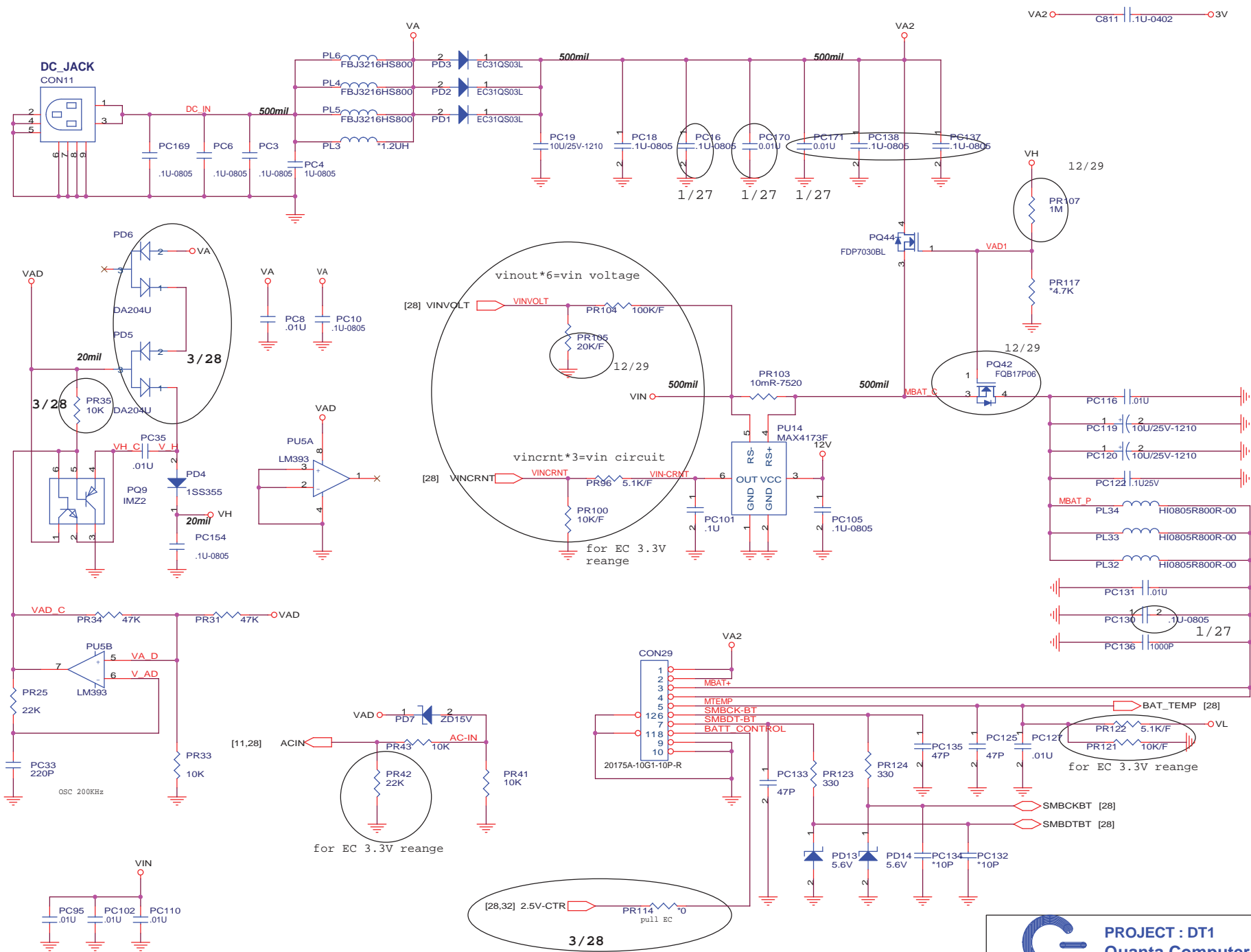


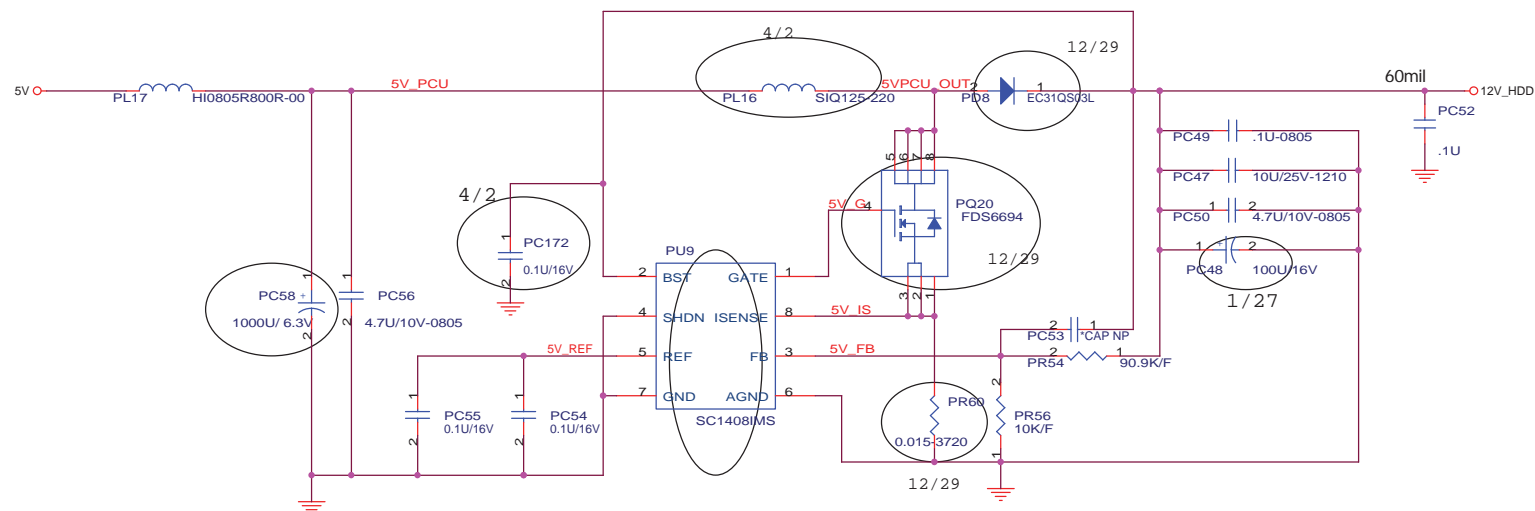
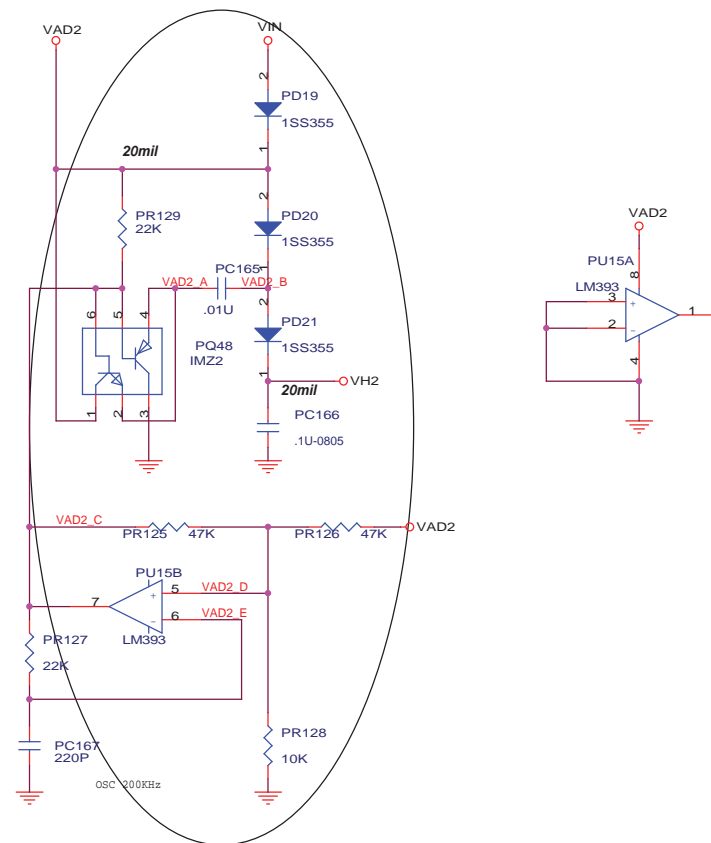
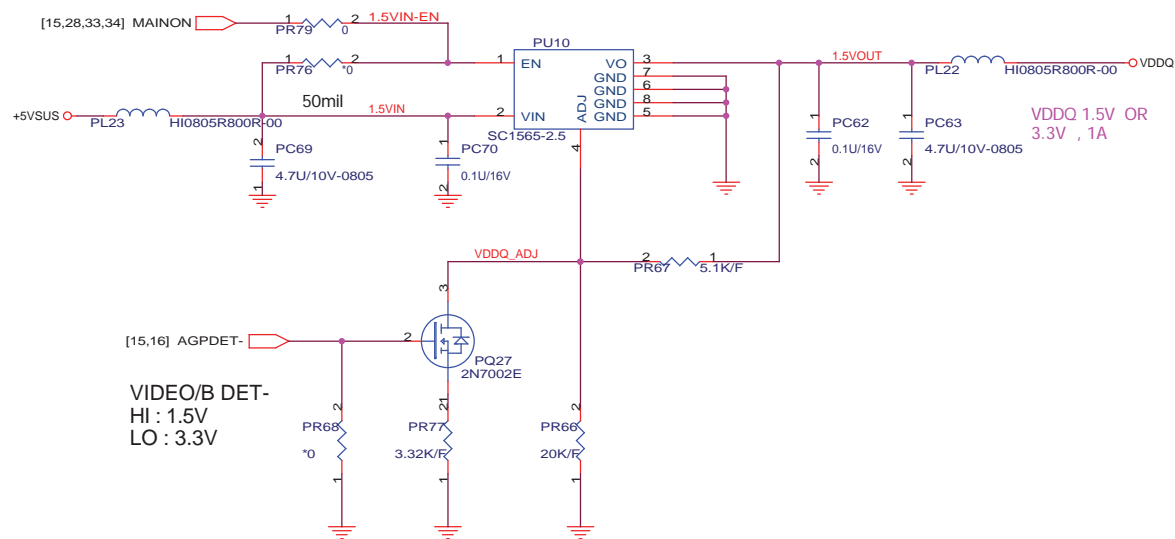
PROJECT : DT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC W83L950D	E
Date:	Friday, April 04, 2003	Sheet 28 of 35



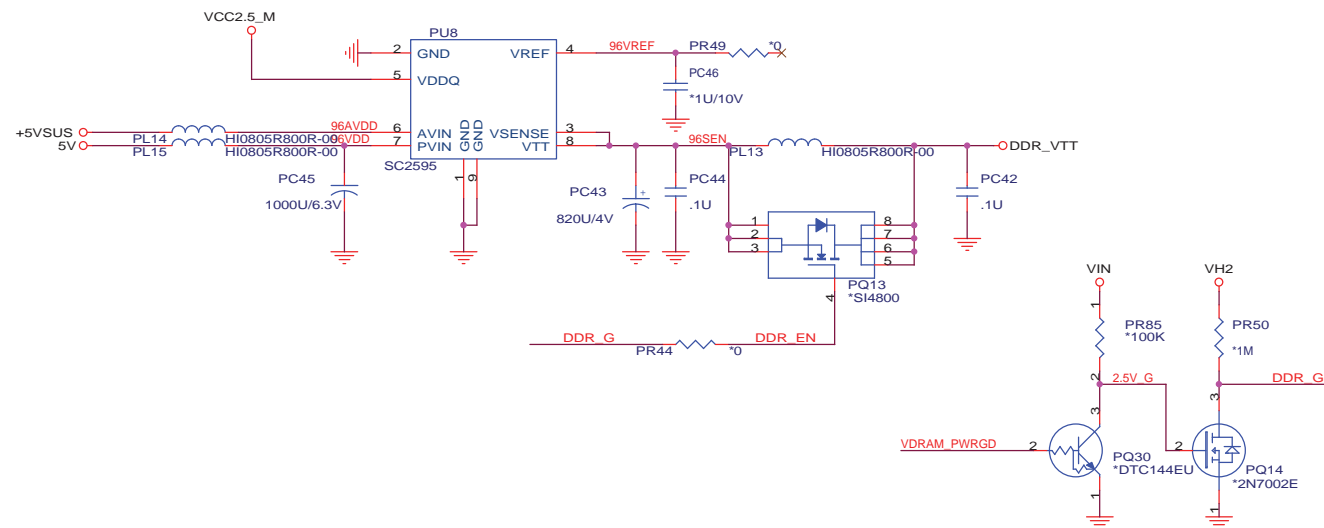
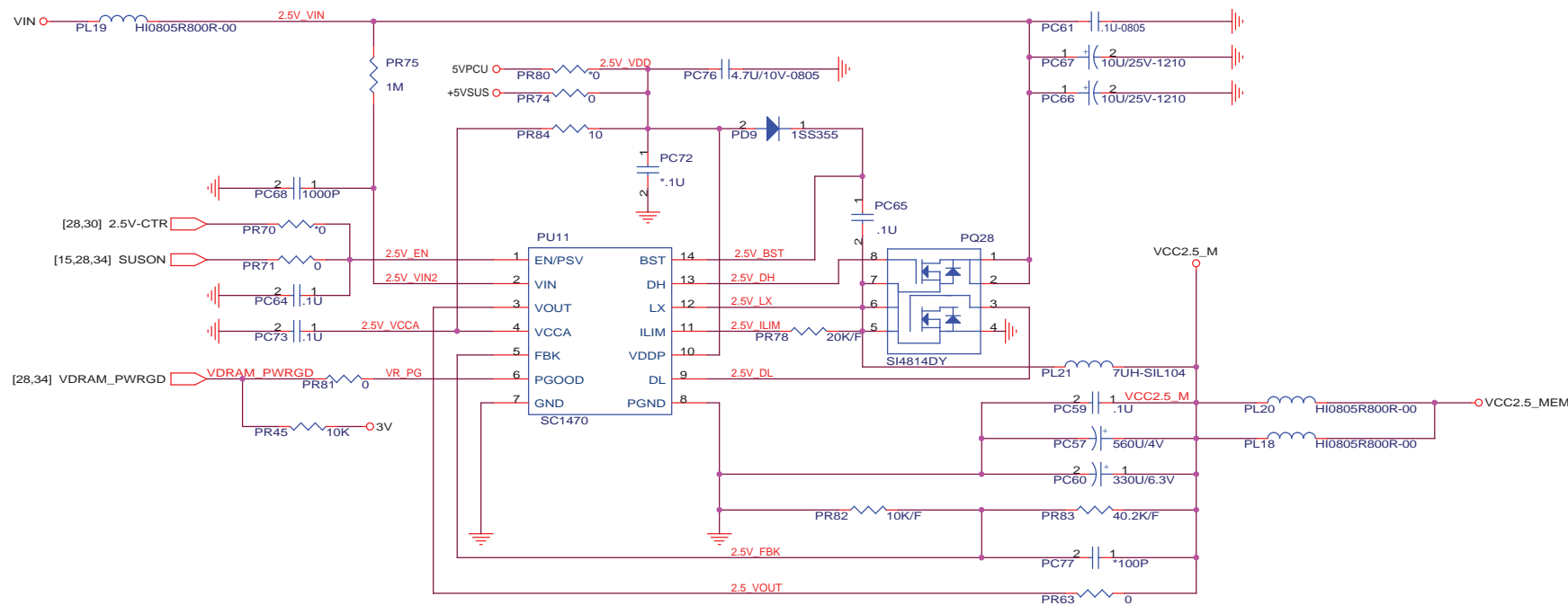
SN74HC148 TABLE													
INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

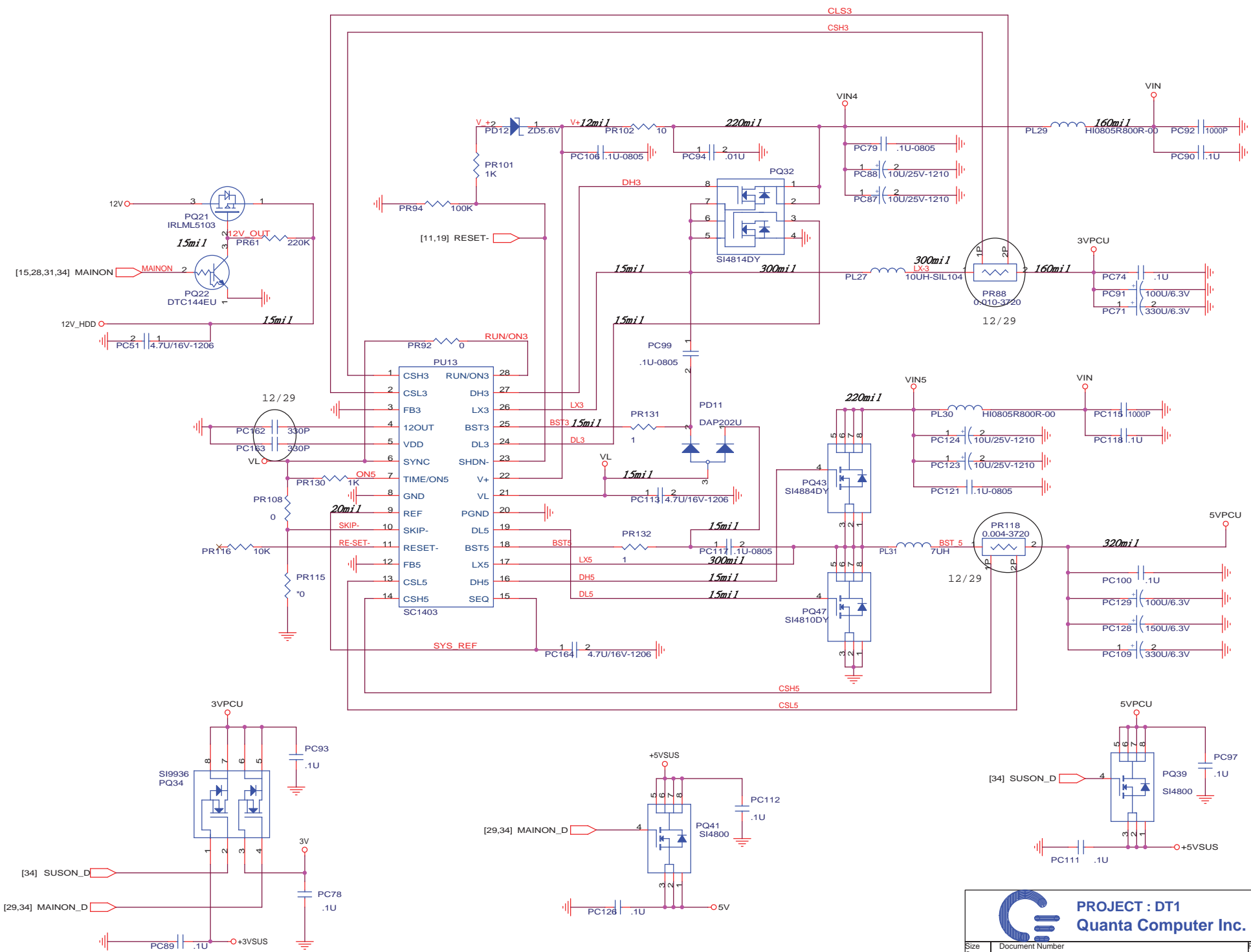




03/06 PC58 CHANGE COMPONENT TO 100U/16V

03/06 PR60 CHANGE FROM 10mohm TO 15mohm





HIP6301 FOR INTEL Brookdale POWER CKT-DDR

